TRANSIENT PROTECTION FOR +7V RAIL

L9 Z=60
C155 u1
C161 100u 25V
TS1 SMBJ10A
DGND
DGND
+7VA
L6 Z=60

J1D Row D
J1C Row C
J1B Row B
J1A Row A

Clock Card - Slot 8

CONFIGURATION READY INTERFACE

+3.3VD
LABEL D4 "nCONFRDY" ON PCB
D4 Red
R1 1k
DEVCLR_holdoff
R2 10k0
R3 470R
FDC6303N Q6B
TO FPGA
CONFRDY
DGND
TP4
Q1B FDC6303N
Q1A FDC6303N
CONF_DONE
DGND

TO FPGA
Q6A FDC6303N
DGND
lvds_rx0bp
lvds_rx0bn
lvds_rx2bp
lvds_rx2bn
lvds_rx4bp
lvds_rx4bn
lvds_rx6bp
lvds_rx6bn
lvds_sparep
lvds_spare n

TO FPGA
SID0
SID1
SID2
SID3
EXTND

J2D Row D
+4.5Vd
+2.5Vd
DGND

J2C Row C
+4.5Vd
+2.5Vd
TO FPGA
lvds_rx0ap
lvds_rx0an
lvds_rx2ap
lvds_rx2an
lvds_rx4ap
lvds_rx4an
lvds_rx6ap
lvds_rx6an
lvds_cmdp
lvds_cmdn
SPTTL2
SPTTL3
DGND

ArryID0
ArryID1
ArryID2
BoxID

J2B Row B
+4.5Vd
+2.5Vd
lvds_rx1bp
lvds_rx1bn
lvds_rx3bp
lvds_rx3bn
lvds_rx5bp
lvds_rx5bn
lvds_rx7bp
lvds_rx7bn
lvds_syncp
lvds_syncn
PSC_MISO
PSC_SREQ
PSC_SPI
TO FPGA
PSC_MOSI
PSC_CCSS
PSC_SCLK
DGND

J2A Row A
+4.5Vd
+2.5Vd
lvds_rx1ap
lvds_rx1an
lvds_rx3ap
lvds_rx3an
lvds_rx5ap
lvds_rx5an
lvds_rx7ap
lvds_rx7an
lvds_clkp
lvds_clkn
TCK
BUSTDI
TMS
BCIr
DGND

BRST

LOCAL RESET BUTTON
SW3
BAS70-04 D6B
D6A BAS70-04
R4 10k0
R134 100R
DGND
+1.5VD
+3.3VD
1.5V LOGIC RESET
U3 MAX6301CSA
RST IN VCC SRT RST SWT WDI GND WDS
C56 u01
C3 u1
R7 47k
R8 36k
RE-CONFIG
3.3V LOGIC RESET/WATCHDOG
U4 MAX6301CSA
C4 1u
C5 u33
C6 u1
R5 10k0
R6 10k0
TP5
nRESET
U1D SN74ALVC126D
FROM FPGA
WDOG

BACKPLANE RESET DETECTOR
R12 24k
R14 15k
U6A LM393M
C8 1n
C9 1n
R16 10k0
R17 10k0
R18 100k
D7A BAS70-04
D7B BAS70-04
+7VA
R139 4k75
R19 1k
C10 u1
R142 2k2
R165 1k
U6B LM393M
R164 1M
R163 1k
nPLUS7VOK

GROUND TO DISABLE WATCHDOG
FROM FPGA
JP1
CONF_DONE
JMPR
R11 100k
INVERTER
Q2A FDC6303N
Q2B FDC6303N

SEE NOTE 3 ON P13-34, STRATIX MANUAL, VOL2 FOR PIN6
JTAG Header P1
GND TCK Vcc TDO NC TMS EN NC GND TDI
R26 220R
R25 100k
R21 100k
R28 1k
FRONT JTAG

JTAG SELECT CIRCUIT
U1A SN74ALVC126D
U2A SN74ALVC125D
U1B SN74ALVC126D
U2B SN74ALVC125D
U1C SN74ALVC126D
U2C SN74ALVC125D
U43A U43B U43C U43D
FPGA_TCK
FPGA_TDO
FPGA_TMS
BB_TCK
BB_TDO
BB_TMS
TCK
TMS
R20 1k
R22 220R
R23 220R
R27 220R
R117 33R
R186 33R
R187 33R
R188 100R
BUSTDO
TO FPGA
nBB_JTAG
FROM FPGA
JTAG_SEL
R13 1k
R15 1k
JTAG DEBUG
P5
JTAG STATE INDICATOR
LABEL D5 "BB_EN" ON PCB
D5 Red
R10 10k0
R9 470R
Q3B FDC6303N
Q3A FDC6303N
C1 u1
C2 u01
C67 u1
C66 u01
U43E SN74ALVC125D
U2D SN74ALVC125D

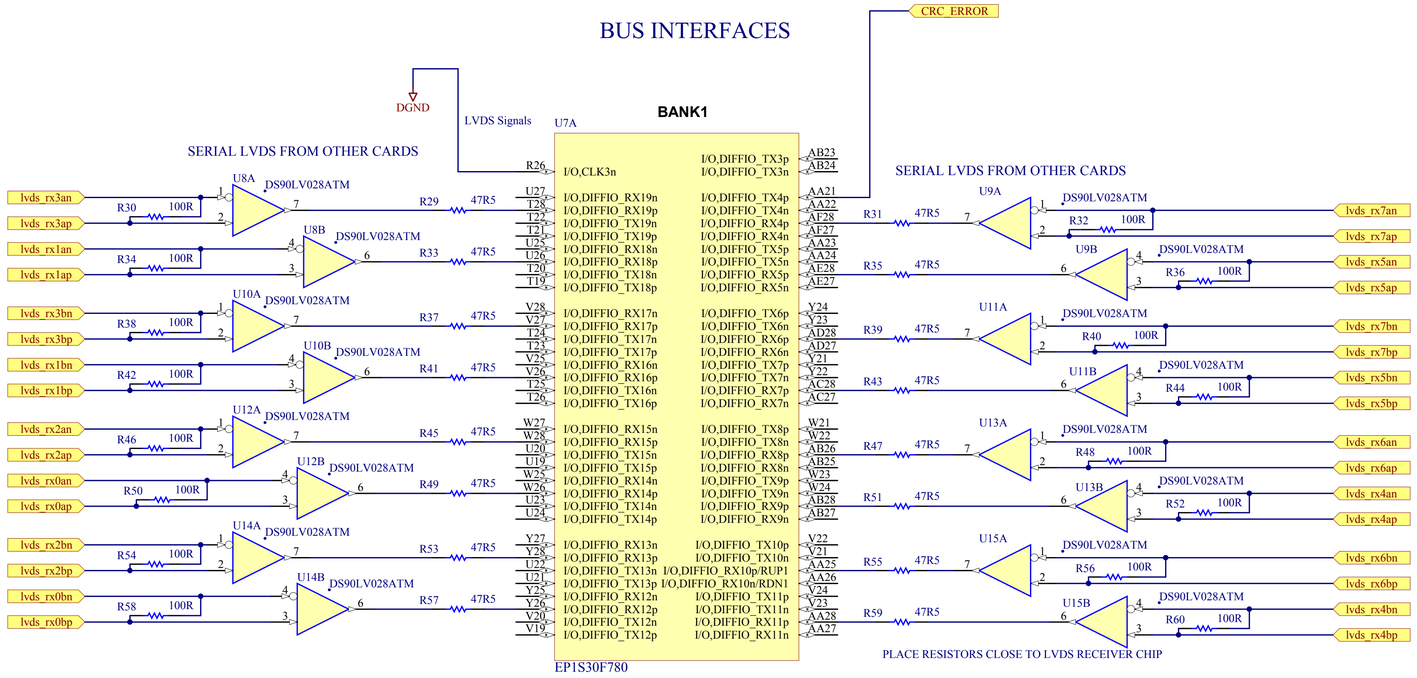
RN53 10k
SW1
SW2
dip_sw2
dip_sw3
dip_sw4
dip_sw5
dip_sw6
dip_sw7
dip_sw8
4 Pos DIP Switch

SW1: ENABLES BYTEBLASTER WHEN CLOSED (FORCES USE OF FRONT PANEL JTAG)
SW2: FPGA OPTION 1
SW3: FPGA OPTION 2
SW4: FPGA OPTION 3

4 Pos DIP Switch
MSEL2: LOW=STANDARD, HIGH=REMOTE/LOCAL
RUnLU: LOW=LOCAL, HIGH=REMOTE

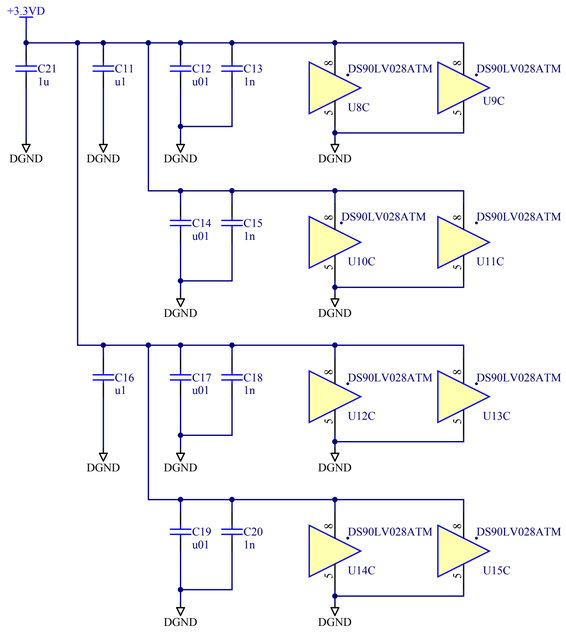
Title: *Clock Card Backplane & Supervisory*		University of British Columbia Department of Physics & Astronomy MCE Project 6224 Agricultural Road Vancouver BC V6T 1Z1 Canada	
Size: B	Number: ELE_S581_101	Revision: C Issue 0	
Date: 2011-11-28 Time: 10:58:37 AM		Sheet 1 of 10	
File: C:\Dynatare\MCEv2\MCEv2 Electronics\MCEv2_Clock_Card\C581-101_S001_BUS.SCHDOC			

BUS INTERFACES



PLACE RESISTORS CLOSE TO LVDS RECEIVER CHIP

LVDS RECEIVERS NEED NOT BE CLOSE TO BACKPLANE CONNECTOR



Title: *Clock Card LVDS Bus Interface*			**University of British Columbia**
Size: C	Number: ELE_S581_101	Revision: C Issue 0	*Department of Physics & Astronomy*
Date: 2011-11-28 Time: 10:58:38 AM		Sheet 2 of 10	*MCE Project*
File: C:\Dynatare\MCEv2\MCEv2 Electronics\MCEv2_Clock_Card\C581-101_S002_LVDS.SCHDOC			*6224 Agricultural Road*
			Vancouver BC V6T 1Z1 Canada

NOTES:

1. DNP = DO NOT POPULATE.

TO FPGA
C_D[7..0]
CLK
C_DCLK
FROM FPGA
nRECONF
nEPC_SEL
TO FPGA
C_OE
nC_CONF
TWEAK R61
PLACE CAPS WITHIN 1.5 INCHES OF POWER PINS
U16
EPM3128ATC100-10
nCF_CONF
nCA_CONF
EP_TDO
M_TDO
F_TCK
F_TMS
DEBUG IO HEADER
HEADER 1X8
ECS-3953M
100MHz
nRESET
SEE NOTE 3 ON P13-34, STRATIX MANUAL, VOL2 FOR PIN6
JTAG Header
FACTORY JTAG
APPLICATION CONFIGURATION
Altera EPC16
Enhanced Configuration Device
BUSTDO
EPC_TDO
TMS
TCK
CONF_DONE
TO FGPA
FACTORY CONFIGURATION
U18
nFLASH_RP
nFLASH_WE
FLASH_ADDR[20..0]
FROM FPGA FLASH INTERFACE
TO FPGA FLASH INTERFACE
FLASH_DQ[15..0]
FLASH_PGM[2..0]
nFLASH_BY
nFLASH_OE
nFLASH_CE
POWER ON RESET CONTROL:
0V = 100 mS
3.3V = 2 mS
CRITICAL_ERROR
CRC_ERROR
delayed_DEVCLR_holdoff
RE-CONFIG
LM393MA
LM393M
FDC6305N
BAS70-04
FDC6303NA
FDC6303N

Title	*Clock Card FPGA Configuration*
Size: B	Number: ELE_S581_101
Revision:	C Issue 0
Date: 2011-11-28	Time: 10:58:38 AM
Sheet 3 of 10	
File:	C:\Dynatare\MCEv2\MCEv2 Electronics\MCEv2_Clock_Card\C581-101_S003_CONFIG.SCHDOC

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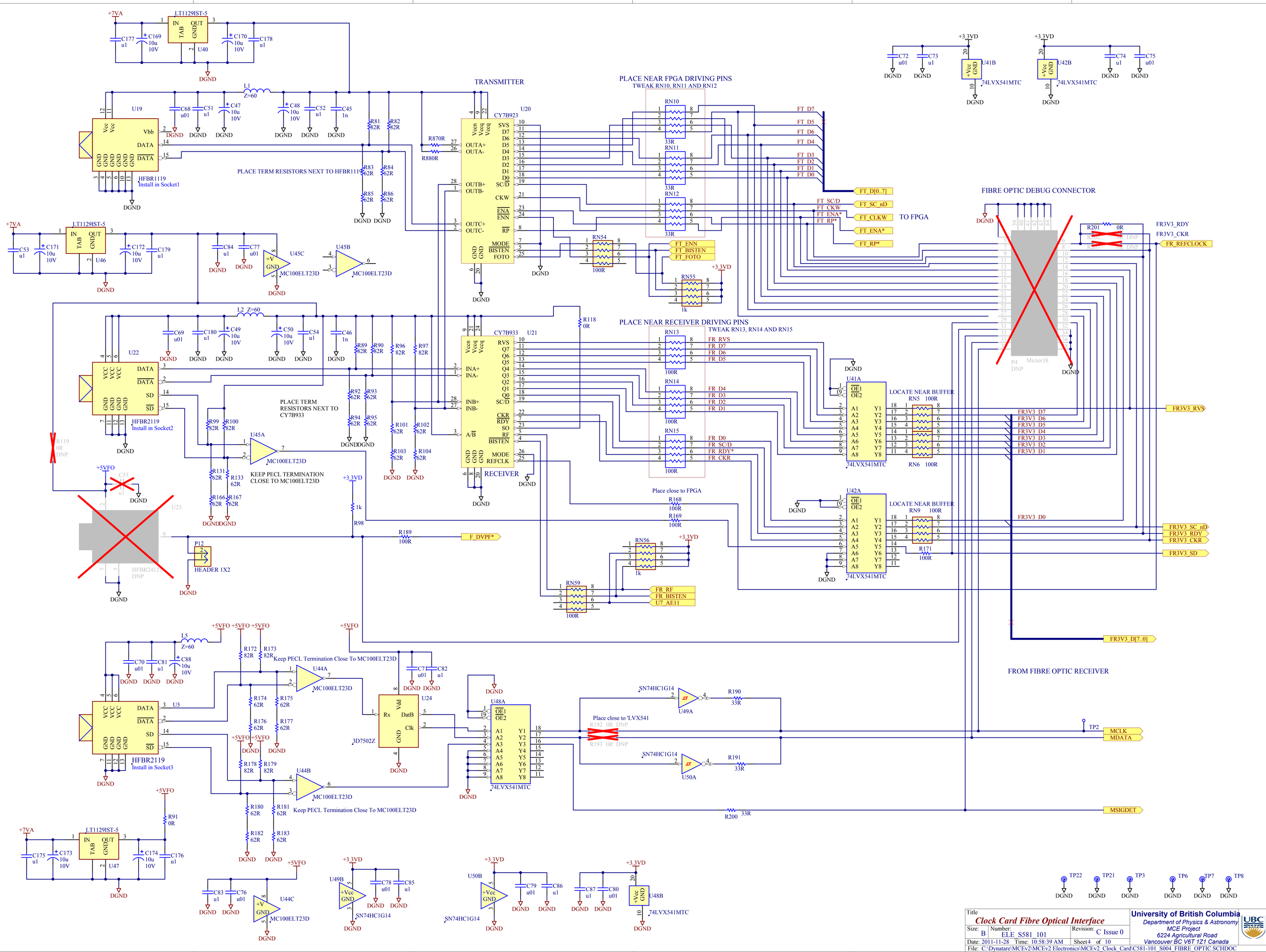
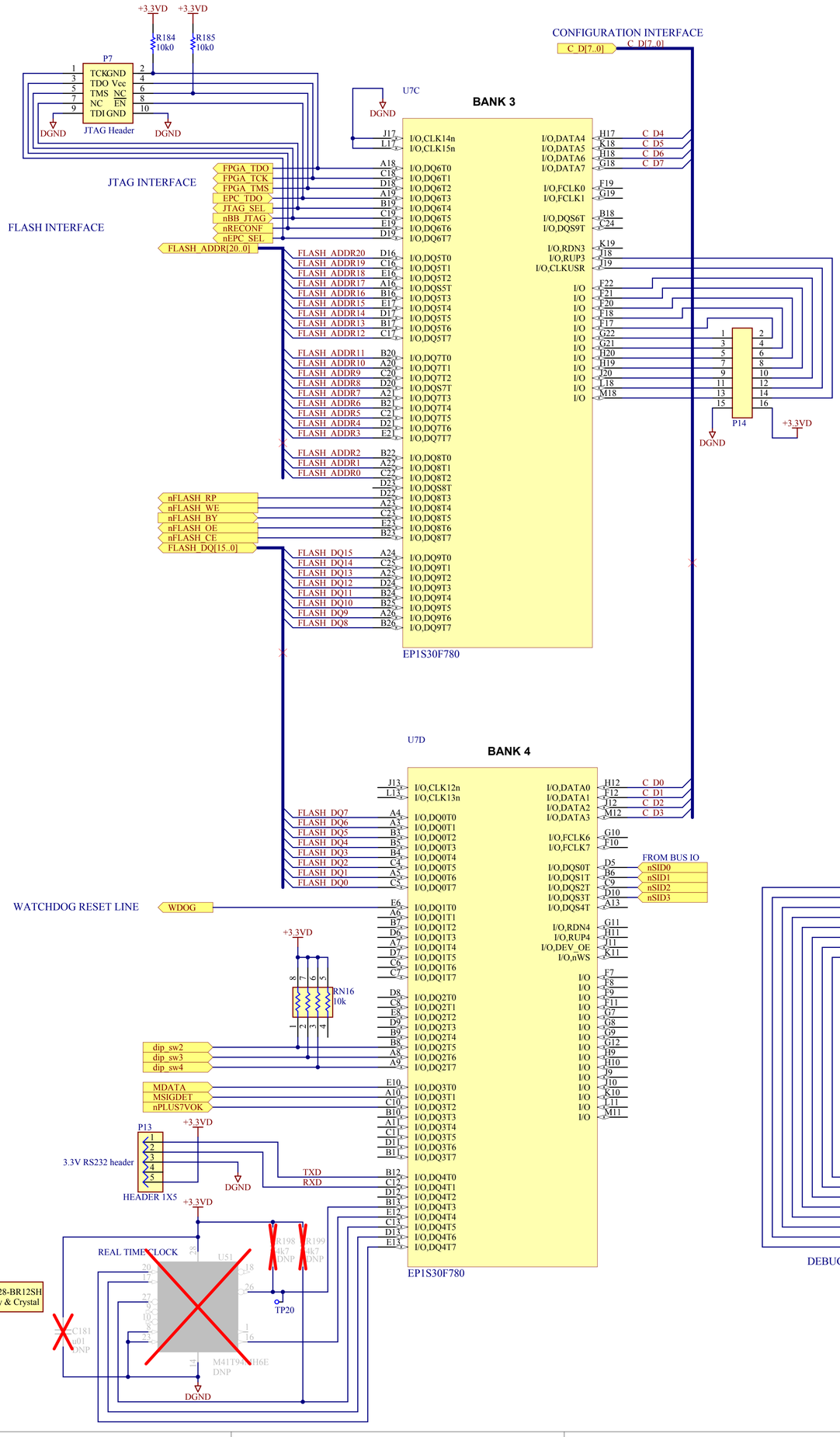
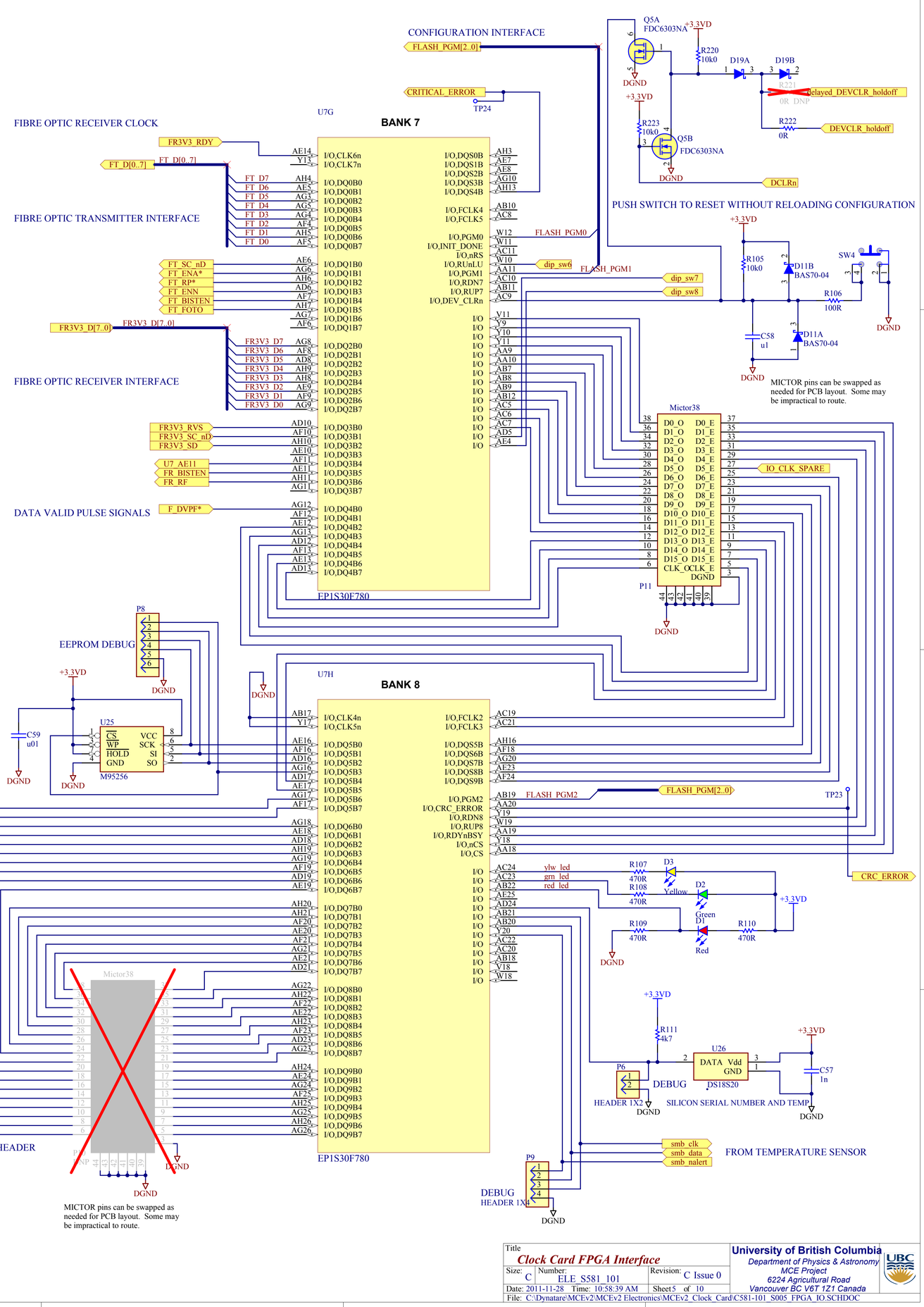

TRANSMITTER
PLACE NEAR FPGA DRIVING PINS
TWEAK RN10, RN11 AND RN12
PLACE TERM RESISTORS NEXT TO HFBR1119
HFBR1119
Install in Socket1
TO FPGA
FIBRE OPTIC DEBUG CONNECTOR
PLACE NEAR RECEIVER DRIVING PINS
TWEAK RN13, RN14 AND RN15
PLACE TERM RESISTORS NEXT TO CY7B933
HFBR2119
Install in Socket2
KEEP PECL TERMINATION CLOSE TO MC100ELT23D
RECEIVER
LOCATE NEAR BUFFER
Place close to FPGA
FROM FIBRE OPTIC RECEIVER
Keep PECL Termination Close To MC100ELT23D
HFBR2119
Install in Socket3
Place close to 'LVX541
HEADER 1X2
Clock Card Fibre Optical Interface
University of British Columbia
Department of Physics & Astronomy
MCE Project
6224 Agricultural Road
Vancouver BC V6T 1Z1 Canada
Size: B
Number: ELE_S581_101
Revision: C Issue 0
Date: 2011-11-28 Time: 10:58:39 AM
Sheet4 of 10
File: C:\Dynatare\MCEv2\MCEv2 Electronics\MCEv2_Clock_Card\C581-101_S004_FIBRE_OPTIC.SCHDOC





Title	*Clock Card FPGA Interface*
Size: C	Number: ELE_S581_101
Revision: C Issue 0	
Date: 2011-11-28 Time: 10:58:39 AM	Sheet5 of 10
File: C:\Dynatare\MCEv2\MCEv2 Electronics\MCEv2_Clock_Card\C581-101_S005_FPGA_IO.SCHDOC	

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Department of Physics & Astronomy
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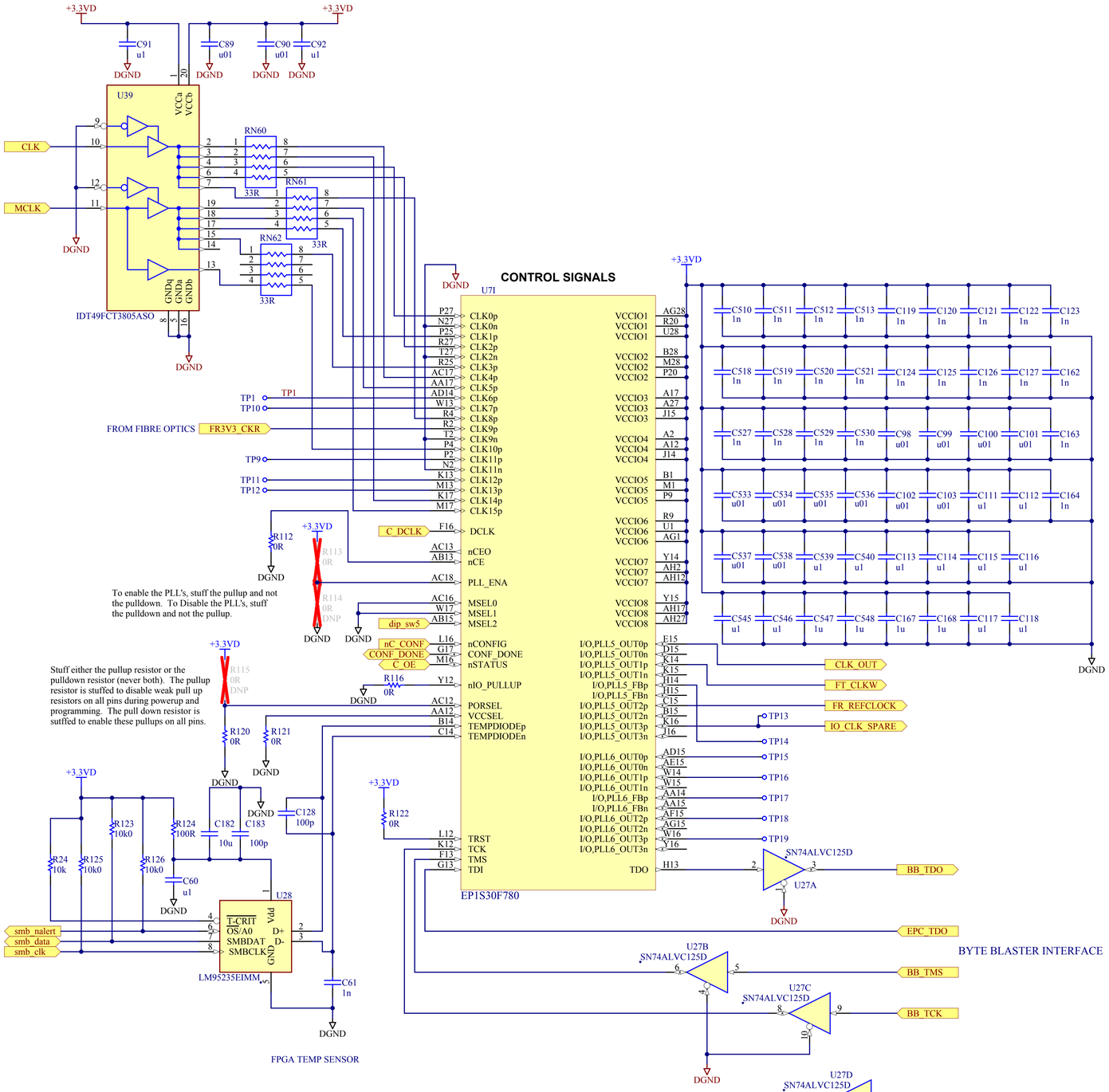
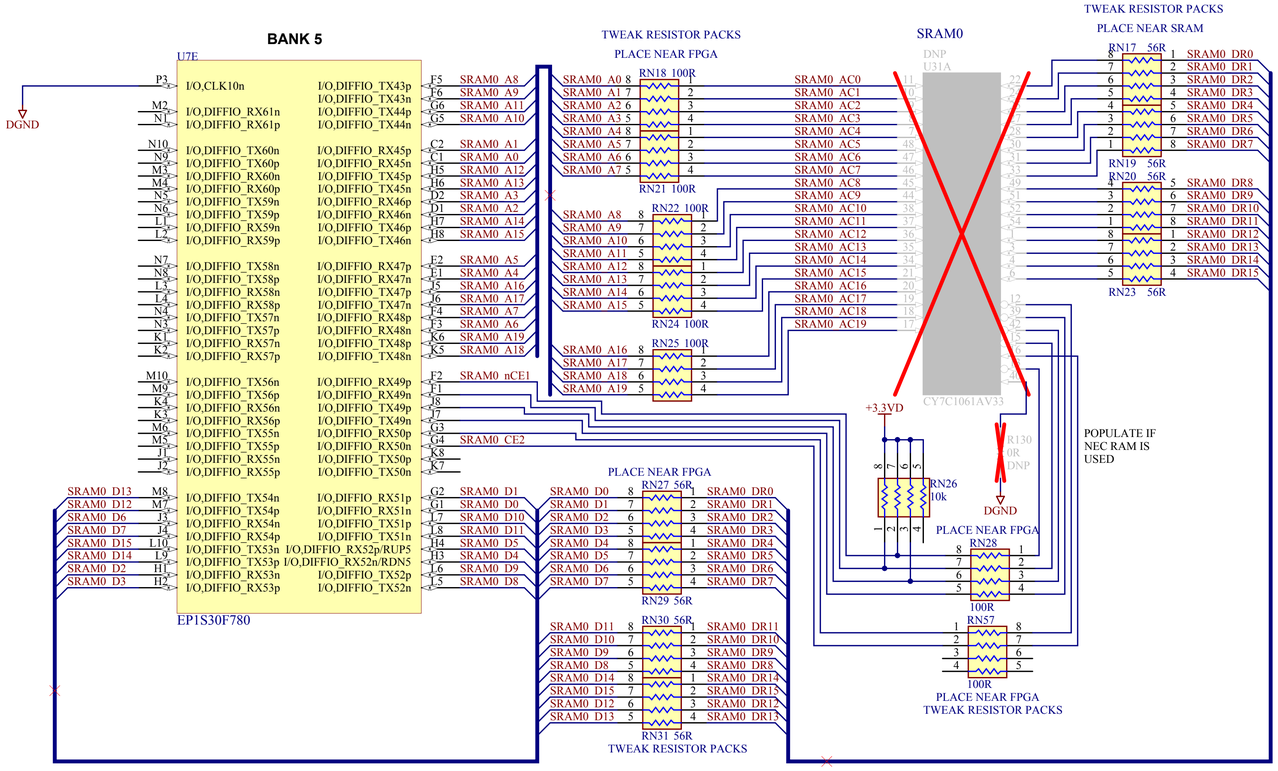
Vancouver BC V6T 1Z1 Canada

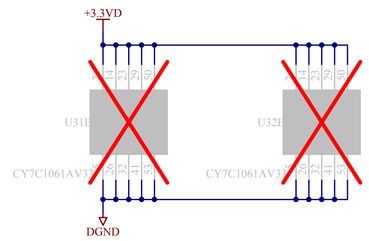


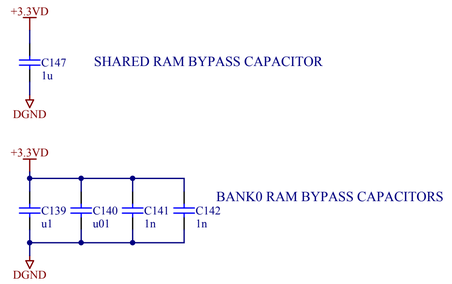
Title	*Clock Card FPGA Power & Decoupling*
Size: B	Number: ELE_S581_101
Revision: C Issue 0	
Date: 2011-11-28 Time: 10:58:40 AM	Sheet 6 of 10
File: C:\Dynatare\MCEv2\MCEv2 Electronics\MCEv2_Clock_Card\C581-101_S006_FPGA_PWR.SCHDOC	

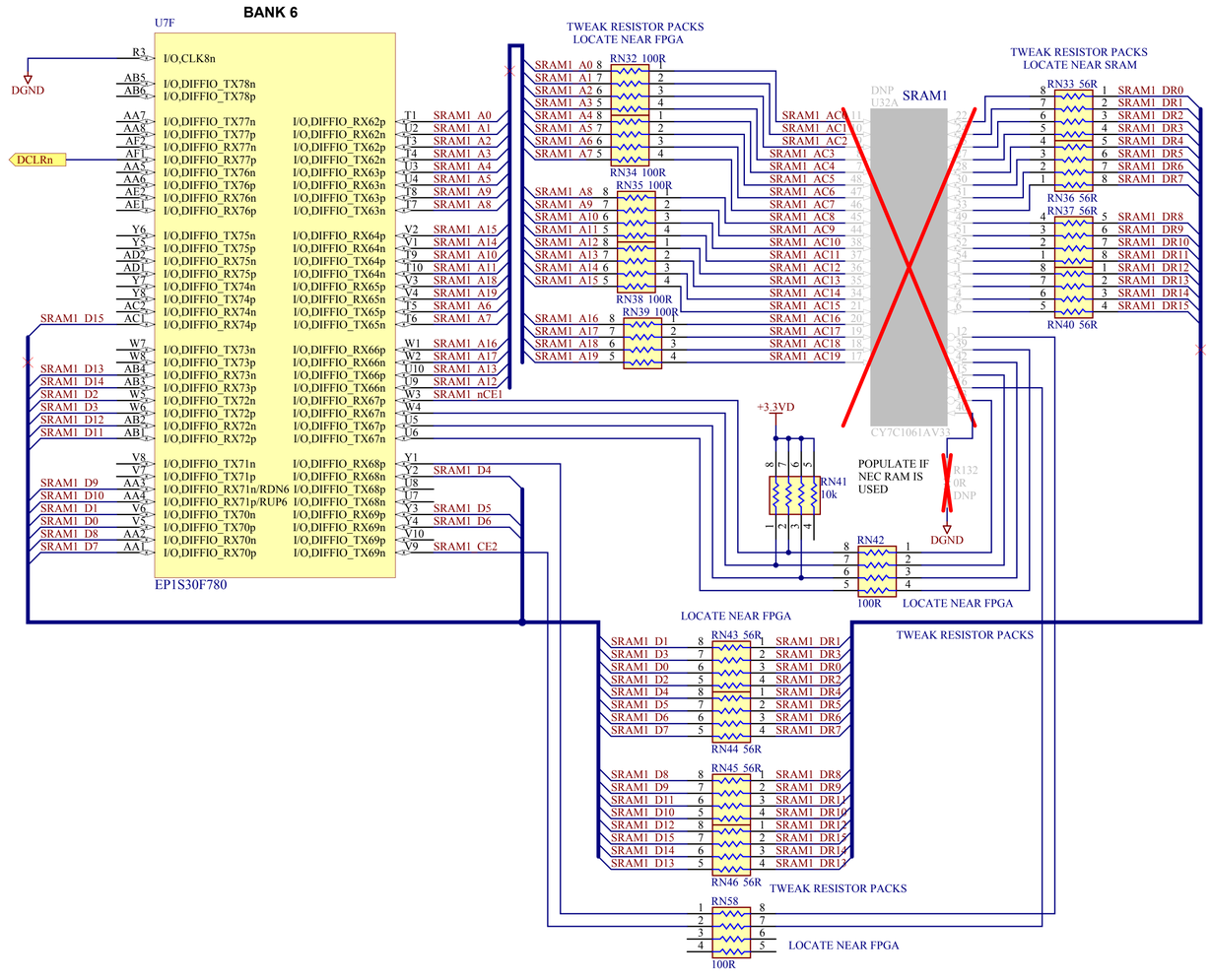
University of British Columbia
Department of Physics & Astronomy
MCE Project
6224 Agricultural Road
Vancouver BC V6T 1Z1 Canada

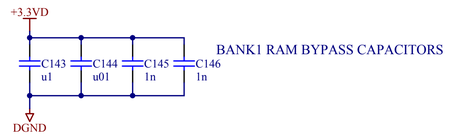
Cannot open file H:\public_html\sc



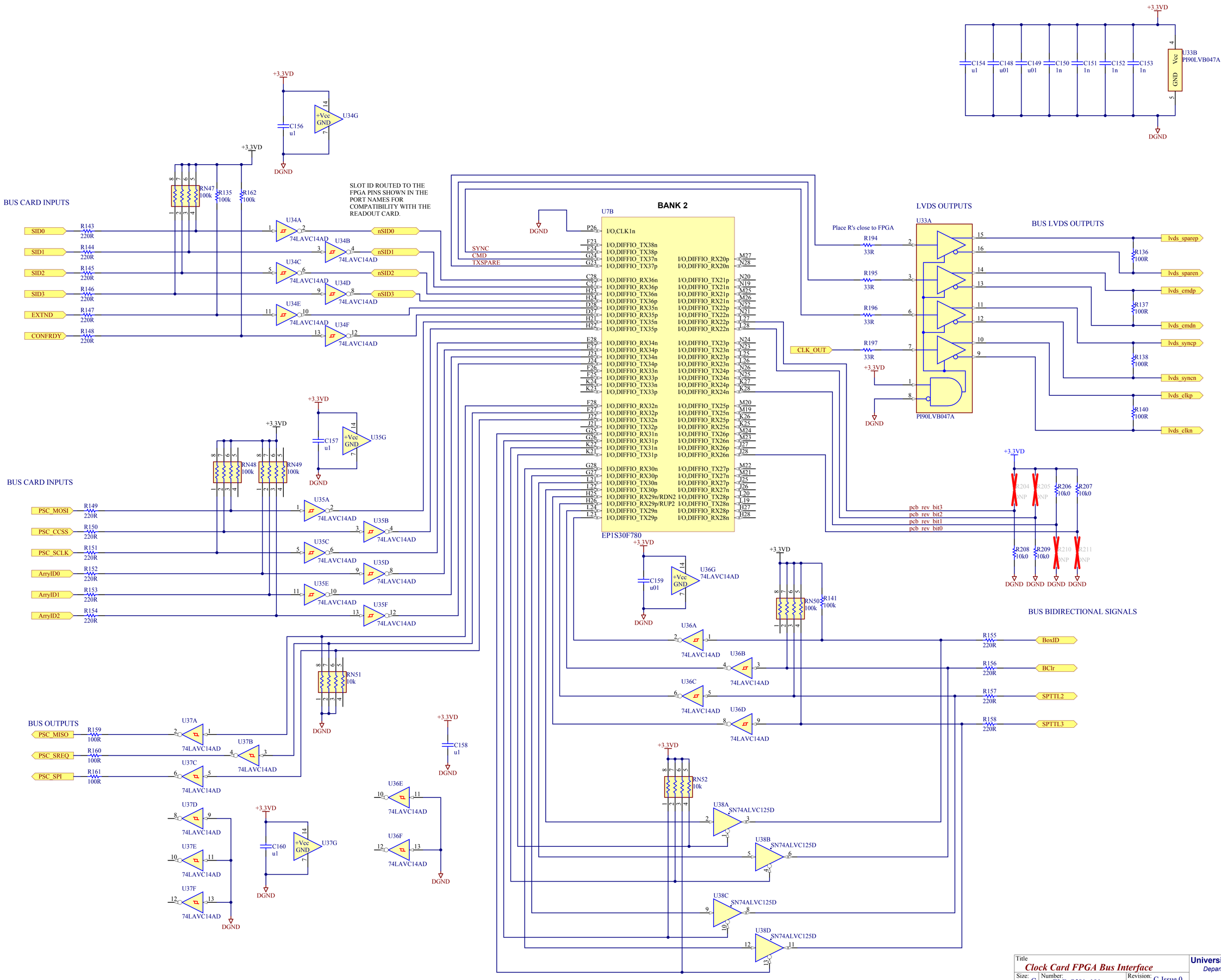








Title	*Clock Card FPGA Memory Interface*		University of British Columbia *Department of Physics & Astronomy* *MCE Project* *6224 Agricultural Road* *Vancouver BC V6T 1Z1 Canada*
Size: C	Number: ELE_S581_101	Revision: C Issue 0	
Date: 2011-11-28 Time: 10:58:40 AM	Sheet 7 of 10		
File: C:\Dynatare\MCEv2\MCEv2 Electronics\MCEv2_Clock_Card\C581-101_S007_SRAM.SCHDOC			



Title	*Clock Card FPGA Bus Interface*
Size: C	Number: ELE_S581_101
Revision: C Issue 0	
Date: 2011-11-28 Time: 10:58:41 AM	Sheet 8 of 10
File: C:\Dynatare\MCEv2\MCEv2 Electronics\MCEv2_Clock_Card\C581-101_S008_FPGA_BUSIO.SCHDOC	

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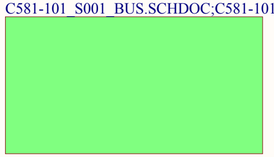
Department of Physics & Astronomy
MCE Project
6224 Agricultural Road
Vancouver BC V6T 1Z1 Canada

SHEET 1
C581-101_S001_BUS.SCHDOC;C581-101_S002_LVDS.SCHDOC;C581-101_S003_CONFIG.SCHDOC;C581-101_S004_FIBRE_OPTIC.SCHDOC;C581-101_S005_FPGA_IO.SCHDOC;C581-101_S006_FPGA_PWR.SCHDOC;C581-101_S007_SRAM.SCHDOC;C581-101_S008_FPGA_BUSIO.SCHDOC;C581-101_S009_MECH.SchDoc



Issue 0

Title: *Clock Card Top Level*			**University of British Columbia** *Department of Physics & Astronomy* *MCE Project* *6224 Agricultural Road* *Vancouver BC V6T 1Z1 Canada*
Size: B	Number: ELE_S581_101	Revision: C	
Date: 2011-11-28 Time: 10:58:41 AM		Sheet 9 of 10	
File: C:\Dynatare\MCEv2\MCEv2 Electronics\MCEv2_Clock_Card\C581-101_S000_TOP.SCHDOC			

TO-220 Heatsink Assembly

M3 x 10mm SSPHMS
Type: Hardware
Manufacturer: Pacific Fastener
Part Number:
Mech1

3mm SS Hex Nut
Type: Hardware
Manufacturer: Pacific Fastener
Part Number:
Mech2

3mm Int Star Lock Washer
Type: Hardware
Manufacturer: Pacific Fastener
Part Number:
Mech5

3W TO-220 Heatsink
Manufacturer: Wakefield
Part Number: 273AB
HS1

Mechanical Part Add to BOM:
Use Heatsink Compound
002096 MEC

See Drawing MEC-C580-195 - Simple Regulator HS Mounting

16 Pin DIP IC Socket
Manufacturer: Mill-Max
Part Number: 110-93-316-41-001
Socket1

16 Pin DIP IC Socket
Manufacturer: Mill-Max
Part Number: 110-93-316-41-001
Socket2

16 Pin DIP IC Socket
Manufacturer: Mill-Max
Part Number: 110-93-316-41-001
Socket3

8 Pin 2x4 0.1"
Manufacturer: Mill-Max
Socket4

Note for Socket 4:

8 Pin 2x4 0.1" Header Machined Pins with manuf # modified from 410-93-210-41-001

Front Panel Mouting Assembly

Bottom Extraction Handle
Manufacturer: Rittal
Part Number: 3686-902
Mech3

Top Extraction Handle
Manufacturer: Rittal
Part Number: 3686-903
Mech4

SCUBA2 Clock Card Front Panel
Manufacturer: PHAS-MS
Part Number: SC2-ELE-S581-110
Mech8

Mechanical Part Add to BOM:
SC2-MEC-S581-111
000655 MEC
Fiber Optic Spacer Plate
Mech7

Mounting Bracket for PCB
Manufacturer: Rittal
Part Number: 3685-198 (10/pack)
Mech11

Mounting Bracket for PCB
Manufacturer: Rittal
Part Number: 3685-198 (10/pack)
Mech12

M2.5 x 8mm Machine Screw Cone Head
Type: Hardware
Mech15

M2.5 x 8mm Machine Screw Cone Head
Type: Hardware
Mech16

M2.5 x 8mm Machine Screw
Type: Hardware
Mech19

M2.5 x 8mm Machine Screw
Type: Hardware
Mech20

M2.5 x 8mm Machine Screw
Type: Hardware
Mech21

M2.5 x 8mm Machine Screw
Type: Hardware
Mech22

Use UBC Logo
Use UBC Logo
PCB Part Number for BOM: ELE-S581-101

Title: *Clock Card Mechanical Hardware*			**University of British Columbia** *Department of Physics & Astronomy* *MCE Project* *6224 Agricultural Road* *Vancouver BC V6T 1Z1 Canada*
Size: B	Number: ELE_S581_101	Revision: C Issue 0	
Date: 2011-11-28 Time: 10:58:41 AM		Sheet 10 of 10	
File: C581-101_S009_MECH.SchDoc			