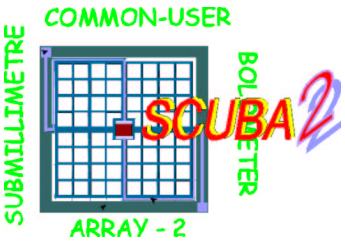

Doc No:	SC2/MCE/sxxx/xxx
Vers:	1.0
Category:	Electronics Analysis
Doc Type:	LaTeX
State:	Revised
Author:	Mark Halpern
Date:	August 11, 2005

Timing and response to Data Valid Pulses

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Summary An auxiliary synchronization circuit for the Multi Channel Electronics (encodes Data Valid signals into a 25MHz clock which optionally synchronizes the separate boxes. If the upon receipt of the encoded signal, the clock card within each box generates commands to slave cards to double buffer the filtered detector signals and then to send this data to the clock card. The clock card also generates an address synch pulse for use by the slave cards. The timing latency is documented. The timing jitter conforms with previous analysis. It is 15μs rms under nominal operation.

Introduction During"Dream" mode, the telescope will generate Data Valid Pulses which are keyed to mirror position and data from the bolometers should be returned with low timing jitter with respect to those pulses. Timing latency, *ie* delay, without jitter is not a serious issue. It is possible in "Scan" mode that a single command would result in collection of many minutes of data with no use of the Data Valid signal for timing but the likely scenario is that in scan mode too data are returned from the MCE in response to a falling edge in the Data Valid signal.

This document presents timing diagrams showing how the presence of a Data Valid signal is detected and communicated to the slave cards in each box of the Multi Channel Electronics. A single box, external to the array control electronics, generates a 25 MHz clock which is communicated via eight separate optical fibres to the eight boxes of control and readout electronics. This external clock allows synchronization of the operation of the boxes. It has been added to the system design in response to suggestions of the PDR review panel. Each box of the control and readout electronics has an internal clock and will operate independently if no external clock is supplied. Upon command the electronics can switch to use the external clock. The timing of address steps and of the address count return-to-zero

are Manchester encoded into the external 25 MHz Clock. See Figure 1.

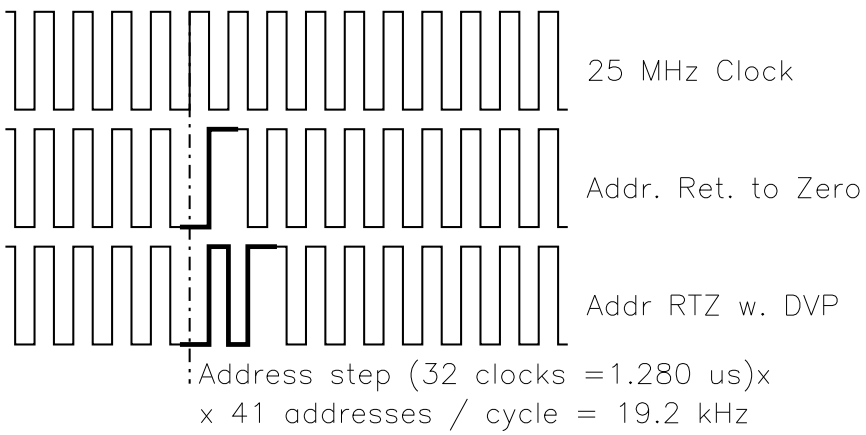

Figure 1: **Manchester Encoding of Address Steps and the Data Valid Pulse:** Every N_ROWS (nominally 41) address steps the address count is returned to zero. The timing of this reset is Manchester Encoded into a 25 MHz clock signal. If a Data Valid signal has been received in the previous 41-step address cycle, this fact is encoded into the Address-Return-to-Zero signal, as shown. Each clock card retrieves the 25 MHz clock, the synch pulse and a data valid pulse from the optical fibre. Whether this external clock or the internal crystal clock is used is controlled by command to the Multi Channel Electronics.

The dwell time at each address is forced to be an integer number of cycles of the 25 MHz system clock. (This forces the system parameter ROW_LEN, the number of 50 MHz clock cycles per address step, to be an even number. I have chosen in illustrations for this document to use $n = 32$, or ROW_LEN=64, which leads to a dwell time of $t_{addr} = 1.280\mu$s, and a frame frequency of 19.05 kHz. This amounts to roughly 95 complete address cycles per anticipated data request since wee anticipate that the Data Valid rate will be 200 Hz.

Each clock card generates a synch pulse to communicate the Address Count Return-to-Zero timing to each slave card in the box. Upon receipt of a Data Valid signal, the Clock Card uses the $41 \times 1.280 = 52.48\mu$s to communicate with slave cards and initiate output from the Infinite Impulse Response filters running on each Readout Card. Processes are running all the time which accumulate several running sums of data from each pixel. During the first full pass through the address order after receipt of a command to return data, each Readout Card combines the accumulated sums with new data to calculate and store filtered output for each pixel. Then the buffer of filtered outputs is returned to the Clock Card on a dedicated line. The timing of this process is shown if Figure 2

This buffering process allows the digital filtering of the data to proceed without interruption and independently of the timing of communication with the Clock Card.

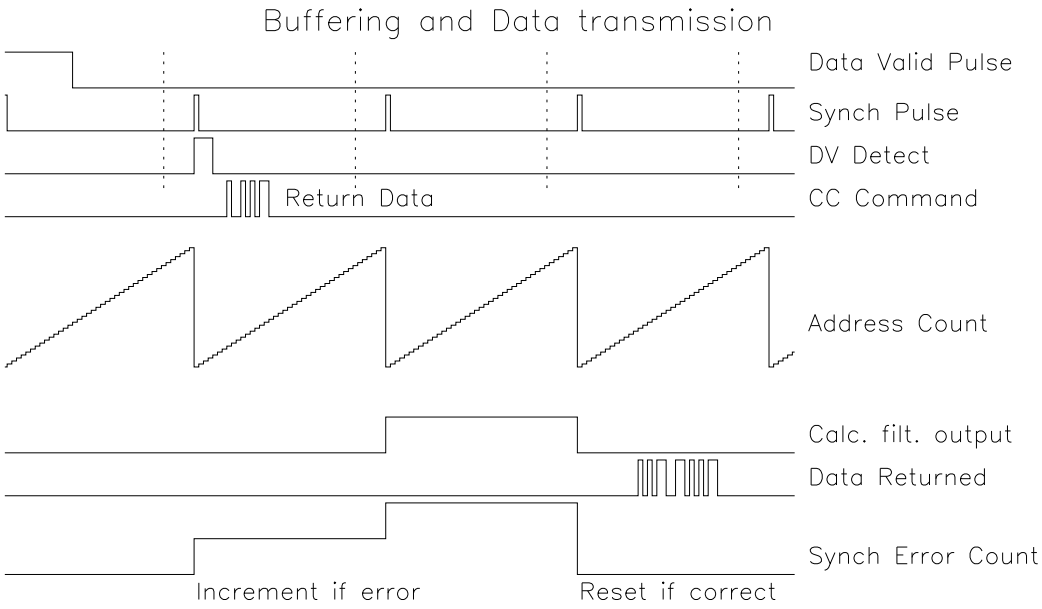

Figure 2: **Filtered Output Timing:** The eight-channel external synch box reads the Data Valid pulse once per address cycle, at the vertical dashed lines. Upon a DV transition to low, DV Detect is manchester encoded and sent to every Clock Card. Before the end of the next address cycle, the Clock Cards command each Readout Card to return data. In the following address cycle filtered outputs are calculated by the IIR filter blocks and returned to the Clock Card via dedicated LVDS lines at the start of the cycle after that. The time between a Data Valid trailing edge and the return of data is uniformly distributed from in the range $2\ 1/2 \pm 1/2$ address cycles.

This filtering and response process introduces a timing latency of into the response to the Data Valid signal. The data are calculated in the second full address cycle after the Data Valid pulse. This latency is uniformly distributed between one and two address cycle times, plus a small offset, for the pixels of row 0. This amounts to latencies from 60 to 112 μs. The filters themselves introduce several millisecond latency so this additional delay is only a few percent of the total and is of no importance whatsoever. There is a new timing *jitter* which arises from waiting for the next Address Count Return-to-Zero, no matter when the Data Valid signal arrives. This jitter is $\delta t = 52.5\mu\text{s}/\sqrt{12} = 15.1\mu\text{s}$. This is an acceptable jitter, as has been pointed out before.

In addition to timing jitter, there is a skew. That is, pixels in row 40 are reported

52 μs later than pixels in row 0. This skew is small–one percent of the width of the filter's impulse response function. As a means of comparison, intrinsic detector time constants are likely to be longer than one ms, so a 5% variation in time constants between pixels produces larger phase shifts than this skew. One strength of this filter design is that this skew, which amounts to a small phase angle between pixels in the recorded data set, is exactly the same in every sample. The small stable phase shift can be handled in data analysis if anyone ever notices it.

Our intended method for synchronizing address cycles is as follows. On each Readout Card and each Address Card, a Synch Error Count is accumulated. This count is incremented by one each time the card's internal address count returns to zero out of synchrony with the Clock Card signal. The count is reset to zero upon any single synchronized Return-to-Zero. If this count reaches some preset value, perhaps 8, the card resets its address counter at the next Return-to-Zero signal. Otherwise each clock relies on its own Address Count. In actual fact, this procedure has not been implemented. The carrds all reset automatically on receipt of the synch pulse. This is as though the preset tolerance level was set to 0.