Physics and Astronomy Dept.
UBC
SCUBA-2 Project

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SC2-ELE-S585-504
Version 7.1

SPI Communications Interface between CC and PS

Revision History:

Rev. 6.0 TF May 08, 2006 Draft

Rev. 7.0 SH Dec. 22, 2006 Finalized to implement firmware

Rev. 7.1 MA Mar. 9, 2007 added headers and rev. history

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The CC and the PS Card communicate via an SPI interface. This interface consists of the following signals:

MOSI – Master Output - Serial output data from the PS Card
MISO – Master Input - Serial input to the PS Card
SCLK – Serial Clock - generated by PS Card
SREQ – Service Request - generated by the CC
CCSS – Clock Card Slave Select - asserted by PS before SCLK for CC data transfers

All transfers are initiated by the CC via the Service Request Signal, SREQ. The PS card provides the SPI clock so it is the SPI "Master". This configuration was chosen as the controller on the PS card already communicates to other devices on the PS card as an SPI Master. The PS Card always has a block of data, as defined in Table 1 below, ready to transmit to the CC. To retrieve the data block the CC asserts SREQ. The PS responds with a 1.5MHz clock burst of 288 cycles (192uS transfer). Data clocked out of the PS Card is read on the rising edge of SCLK. As data is read by the CC on the MOSI line a command is being sent on the MISO line.

Power Command Structure

Commands are either the Request Status command which occurs at a periodic rate, a Subrack Reset or Power Command. Commands from the CC are 2 bytes long. Commands are clocked into the PS card as the data is clocked out. As each data block is 36 bytes and each command is 2 bytes a command may be repeated up to 18 times. To ensure command integrity each command must be sent at least 3 consecutive times. The power supply card checks that at least 3 consecutive commands match then acts upon the command. If all commands match the ACK character (0x60 is inserted in the data buffer otherwise the NAK character is inserted. The common periodic Request Status command is signaled by holding the MISO pin low for the whole 256 cycle clock burst. This is essentially the default command. Other commands use 2 unique ASCII characters for each command. The following commands are defined:

Cycle Power Command

Byte 1 (ASCII 'C")

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	1

Byte 2 (ASCII 'P')

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0

sequence_off()
wait()
sequence_on()

Reset MCE Command

Byte 1 (ASCII 'R")

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	1	0

Byte 2 (ASCII 'M')

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	0	1

BRST = 1
wait()
BRST = 0

Turn Off Command

Byte 1 (ASCII 'T")

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0

Byte 2 (ASCII 'O')

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	1	1

sequence_off()

The SPI clock rate is set to 1.5MHz, but may change. At this rate the Power Supply Controller is be able to determine if a command is valid in time to update the ACK/NAK byte. The check digit for data with ACK and data with NAK will have to be calculated in advance with the correct checksum inserted once the command's validity is determined.

Power Supply Data Block

Byte #s	Item	Bytes	Description
0	Silicon ID	4	32 least sig bits of 48 bit ID
4	Software Version	1	Encoded as hex byte. 0xYZ = version Y.Z
5	Fan1 Tachometer	1	Currently not used
6	Fan2 Tachometer	1	Currently not used
7	PSU Temperature 1	1	8 bit two's compliment (1 deg. increments)
8	PSU Temperature 2	1	8 bit two's compliment (1 deg. increments)
9	PSU Box Temperature 3	1	8 bit two's compliment (1 deg. increments)

10	ADC Offset	2	Digitized Ground (bipolar, 2 bits/deg C)
12	Supply Voltage 1	2	+Vcore Supply – unipolar scaled to 73.2%
14	Supply Voltage 2	2	+Vlvd Supply – unipolar scaled to 73.2%
16	Supply Voltage 3	2	+Vah Supply – unipolar scaled to 73.2%
18	Supply Voltage 4	2	+Va Supply – unipolar scaled to 73.2%
20	Supply Voltage 5	2	-Va Supply – unipolar scaled to 73.2%
22	Supply Current 1	2	Current +Vcore– unipolar scaled to 61%
24	Supply Current 2	2	Current +Vlvd– unipolar scaled to 61%
26	Supply Current 3	2	Current +Vah– unipolar scaled to 61%
28	Supply Current 4	2	Current +Va– unipolar scaled to 61%
30	Supply Current 5	2	Current -Va– unipolar scaled to 61%
32	Status Word	2	For future expansion
34	ACK/NAK	1	ACK if command correct/NAK otherwise
35	Check Digit	1	2's compliment of sum of all other bytes
	Total	36	36 x 8 = 288 clocks on the SPI Interface

Status Word Definition

No bits defined in current implementation:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0

Check Digit

Many methods are possible. Trade-off between computational complexity (and speed) vs. error detection ability.

Current implementation is a checksum to for minimal processor overhead:

```
Sum  = 0                              (1 byte character)
For each byte in Data Block
        Sum = Sum + byte              (Ignoring overflow)
Checkbyte = ~Sum +1                   (2's compliment)
```

Hence on CC receipt of data block. Checkbyte + (all other bytes in datablock) should = 0. A non-zero value here indicates an error.