MCE Communication Protocols

Revision History

Rev	*Date*	*Description of change*
1.0	2007-07-05	Merged previous documents: 1. SPI Communication Interface Between CC and PS [SC2_ELE_S585_504 Rev. 7.1] 2. Bus Backplane ISA [SC2_ELE_S580_511 Rev. D] 3. Fibre_and_backplane_protocols.xls
1.1	2007-08-22	Rewritten parts
1.2	2007-10-22	BB: Added more detail for reply and data packets in section 2
1.3	2012-01-04	Cleaned up the redundant packet descriptions and minor edits

Abstract

This document describes hardware and software standards that govern data transmission between different parts of the system. The protocol outlined here may define the packet structure of the data transmitted or the control commands to manage the communication. This document has multiple sections. The data exchange between the MCE and the outside world is over the fibre-optic link to the controlling PC, over a fibre link to an external synchronization source, or through the front-panel RS232 port for debugging purposes. The inter-card communication within the MCE including the backplane communication is also reviewed. In each case, we describe the physical layer responsible for transferring bits without any understanding of the contents of the bits. Then we describe the data-link layer that is responsible for validity and integrity of the transmission and how a connection is established. Finally, we explain the control commands and data exchanged for each case.

1. General Description

1.1 Background

2. MCE / PC Communication over the Fibre-optic Link

2.1 Physical Layer

The communication between the PC and the MCE is through a duplex fibre-optic link. The fibre-optic receive/transmit circuitry contains Agilent parts HFBR1119/2119 operating in the IR regime at a bit rate of 250MHz, derived from Cypress HotLink, CY923/33, parallel-to-serial and serial-to-parallel converters that synthesize a 250MHz clock from an input clock of 25MHz. HOTLink is an 8B/10B physical layer for point-to-point communication over high-speed serial link with special characters defined, but no HOTLink protocol standard exists. These parts require ten clocks to transmit or receive each byte, so the 250MHz bit rate translates into 25MB/s. On the PC side, a PCI card from San-Diego State University (SDSU) handles data acquisition from the MCE [2]. On the MCE side, Clock-Card (CC) has the fibre interface circuitry (see section 2.4.3 in [1]).

2.2 Data Link Layer

The communication protocol between the data-acquisition PC and the MCE is detailed in [3] "SCUBA-2 Data Acquisition Software Overview – Part two Protocols", SC2/SOF/S200/014,. Packets originating from the PC are referred to as *command* packets and packets originating from the MCE are referred to either as *reply* packets or *data* packets. Each command packet has to be acknowledged by the MCE through a *reply* packet within limited time; if no reply is received then the PC issues a timeout warning and stops waiting. As a general rule, the PC ignores unsolicited *reply* or *data* packets from the MCE. (Consequently, a late *reply* packet is ignored). Each command has to be acknowledged (or timed out) before another command is issued. Packet collision is avoided by the nature of this protocol. There are two special command types:

1. *GO* command: a *reply* packet is followed by one or many *data* packets and the last *data* packet is marked as last (see **Table 4**).

2. *ST* command: one or many *data* packets with last *data* packet marked as last are followed by a *reply* packet.

A packet consists of 32-bit little-endian words. The asynchronous nature of communication requires that all valid packets (*command*/*reply*/*data*) include two 32-bit preamble words (0xA5A5A5A5 followed by 0x5A5A5A5A) to indicate the start of a valid packet. The transmitter inserts a simple XOR checksum as the last word in the packet. The receiver regenerates the checksum based on the packet data and compares it with the one included in the packet to detect bit errors. The simple checksum offers a naive error detection mechanism, but no error correction mechanism exists in the protocol. The decision was made based on low fibre bit-error rates. A bit-error rate (BER) $<10^{-19}$ is measured.

2.3 Packet Structure and Content

There are 3 types of packets exchanged between the MCE and the PC. Tables 1, 2, and 3 detail *command*, *reply*, and *data* packets.

2.3.1 Command Packets

The command packets are 64 words long and contain one of 5 different command types (word 2) as listed here and detailed in [6] "Firmware Overview", SC2_ELE_S500_23, Version 2, *UK Astronomy Technology Centre*:

- RB Read block to read back a parameter from MCE
- WB Write Block to set an MCE parameter
- GO start a (data-acquisition) process on MCE
- ST stop a (data-acquisition) process on MCE
- RS reset command is used to provide different levels of reset in MCE

Word 3 in the command packet specifies an MCE card address and parameter address, while word 5 to 62 data to be written if any. For list of card addresses and parameters refer to [4] "MCE Command Description", SC2_ELE_S580_515.

The packet size, word 4, indicates the number of valid data items. All non-valid data items are set to 0x0 in DAS (Refer to end of section 4.2 in [3] "SCUBA-2 Data Acquisition Software Overview – Part two Protocols", SC2/SOF/S200/014, *UK Astronomy Technology Centre*.) There is one exception for command packets with command type of RB, where packet size is set to number of items to be included in the reply packet instead of number of data items in the command packet!!!

The checksum, word 63, is calculated over all 58 data items (including valid and invalid items).

32-bit Word	Title	Description
0	Preamble 0	0xA5A5A5A5
1	Preamble 1	0x5A5A5A5A
2	Command Type	0x2020xxxxx where xxxx is one of RB/WB/GO/ST/RS
3	Card_ID (16-bit) / Parameter_ID (16-bit)	Refer to [4] for list of Card_Ids and Par_Ids
4	Packet Size (n)	Num. of valid data items 1 ≤ n ≤ 58 for RB/WB commands n = 1 for GO/ST/RS commands
5	Data 0	Valid or 0x0
	…	Valid or 0x0
	…	….
62	Data n-1	Valid or 0x0
63	Checksum	XOR checksum of word 5 to 62

Table 1: Command Packet over the Fibre Link- Fixed size of 64 Words.

2.3.2 Reply Packets

A *reply* packet indicates fail/success (OK/ER) status of the command-packet delivery to MCE and includes the inquired parameter values if any.

The packet type, word 2, is set to " RP" to indicate that this is a *reply* packet as oppose to a *data* packet.

Word 3 specifies the packet size in terms of number of data items + 3. Word 4 indicates the fail/success status of the command. In case of a failure, Word 6 contains the error code.

The MCE card address and parameter address are specified in Word 5. Word 6 and on are reserved for data. (Currently, no MCE parameter has more than 41 data items associated with.)

32-bit Word	Title	Description
0	Preamble 0	0xA5A5A5A5
1	Preamble 1	0x5A5A5A5A
2	Packet Type = RP	0x20205250 or " RP"
3	Packet size = Data Size (n) + 3	1 ≤ n ≤ 58 for RBOK replies n=1 for **non** RBOK replies
4	Reply Type *	XXYY where XX is one of RB/WB/GO/RS YY is one of OK/ER
5	Card_ID (16b) / Parameter_ID (16b)	Refer to [4] for list of Card_Ids and Par_Ids
6	Data 0	first data item for RBOK replies 0x0000 for non RB replies error_number for ER replies
	Data 1	Optional
	….	….
5+n	Data n-1	Optional
6+n	Checksum	XOR checksum of word 4 to 5+n

Table 2: Reply Packet over the Fibre Link

* For example: XXYY for RBOK is 0x52424F4B.

Table 3 lists the bit description for **error_number** word of the reply packet.

Bit Number	Bit Description
31	Stale data
30	Internal reset has occurred
29	Card not present, AC
28	Backplane communications error, AC
27	Wishbone execution error, AC
26	Card not present, BC1
25	Backplane communications error, BC1
24	Wishbone execution error, BC1
23	Card not present, BC2
22	Backplane communications error, BC2
21	Wishbone execution error, BC2
20	Card not present, BC3
19	Backplane communications error, BC3
18	Wishbone execution error, BC3
17	Card not present, RC1
16	Backplane communications error, RC1
15	Wishbone execution error, RC1
14	Card not present, RC2
13	Backplane communications error, RC2
12	Wishbone execution error, RC2
11	Card not present, RC3
10	Backplane communications error, RC3
9	Wishbone execution error, RC3
8	Card not present, RC4
7	Backplane communications error, RC4
6	Wishbone execution error, RC4
5	Card not present, CC
4	Backplane communications error, CC
3	Wishbone execution error, CC
2	Card not present, PSUC
1	Backplane communications error, PSUC
0	Wishbone execution error, PSUC

Table 3 error_number bit description

Strictly speaking, the 'Card Not Present' bits (highlighted in yellow, above) are not errors. In reply packets to the PC, the MCE will assert the bits of all cards that are missing from the MCE, but will not assert the xxER flag, even if the missing card was commanded.

'Backplane communications errors' include CRC errors and timeouts.

'Wishbone execution errors' include attempts to write to read-only parameter IDs (i.e. register), and attempts to access a parameter ID that is not supported by a card's firmware.

2.3.3 Data Packets

As described earlier, commands of type GO are acknowledged by a reply packet followed by a data packet. Word 3 in a data packet specifies DA for packet type. Then word 4 specifies the packet size.

32-bit Word	Title	Description
0	Preamble 0	0xA5A5A5A5
1	Preamble 1	0x5A5A5A5A
2	Packet Type= DA	0x20204441 or " DA"
3	Packet Size = Data Size (n) + 1	
4	Data 0	
…	….	
…	….	
3+n	Data n-1	
4+n	Checksum	XOR checksum of word 4 to 4+n

Table 4: Data Packet over the Fibre Link

The data section of the packet, Data 0 to Data n-1, is referred to as an MCE data frame. It consists of :

- 43 words of header information, documented in Table 5.
- 8*R*N words of data, where N is the number of readout cards reporting and R is the number of rows reporting.
- 1 word of checksum

Data Packet Header				
Word #	Byte 3 31 30 29 28 27 26 25 24	Byte 2 23 22 21 20 19 18 17 16	Byte 1 15 14 13 12 11 10 9 8	Byte 0 7 6 5 4 3 2 1 0
0	**Data Frame Status Bits**			
1	**Clock Card Data Frame Counter**			
2	**Address Dwell Time (row_len)**			
3	**Number of Rows Reported (num_rows-reported)**			
4	**Data Period (data_rate)**			
5	**Clock Card Address Return to Zero Counter**			
6	**Header Version #**			
7	**Ramp Value**			
8	**Ramp Card Address**		**Ramp Parameter ID**	
9	**Number of Rows Servoed**			
10	**Sync Box Number**			
11	**Run ID # (run_id)**			
12	**User Writable (user_word)**			
13	**Errno**			
14	**FPGA Temperature, AC**			
15	**FPGA Temperature, BC1**			
16	**FPGA Temperature, BC2**			
17	**FPGA Temperature, BC3**			
18	**FPGA Temperature, RC1**			
19	**FPGA Temperature, RC2**			
20	**FPGA Temperature, RC3**			
21	**FPGA Temperature, RC4**			
22	**FPGA Temperature, CC**			
23	**Errno**			
24	**Card Temperature, AC**			
25	**Card Temperature, BC1**			
26	**Card Temperature, BC2**			
27	**Card Temperature, BC3**			
28	**Card Temperature, RC1**			
29	**Card Temperature, RC2**			
30	**Card Temperature, RC3**			
31	**Card Temperature, RC4**			
32	**Card Temperature, CC**			
33	**Errno**			
34	**Software Version, PSUC**	**Fan 1 Tachometer, PSUC**	**Fan 2 Tachometer, PSUC**	**Temperature 1, PSUC**
35	**Temperature 2, PSUC**	**Temperature 3, PSUC**	**ADC Offset, PSUC**	
36	**Supply Voltage 1, PSUC**		**Supply Voltage 2, PSUC**	
37	**Supply Voltage 3, PSUC**		**Supply Voltage 4, PSUC**	
38	**Supply Voltage 5, PSUC**		**Supply Current 1, PSUC**	
39	**Supply Current 2, PSUC**		**Supply Current 3, PSUC**	
40	**Supply Current 4, PSUC**		**Supply Current 5, PSUC**	
41	**Errno**			
42	**Box Temperature**			

Table 5 Data Header Information (Version 6) in an MCE Data Frame

3. Communication Protocol over the Backplane

3.1 Physical Layer

The 25Mb/s asynchronous serial communication link over the backplane is carried out over 1 multi-drop LVDS pairs from Clock Card (CC) to other cards (star-link) and point-to-point LVDS pairs from every address card (AC), bias card (BC), and readout card (RC) back to CC for a total of 16 pairs. A 25MHz *sync* clock is generated on CC and distributed to all cards over a backplane LVDS pair. On each card, the *sync* clock is fed to a PLL to generate the receiver clock.

3.2 Data-Link Layer

The backplane communication follows the command-response model where communication is always initiated by CC. The multi-drop line is used to issue commands to other cards. Each card sends a reply back on one of its 2 dedicated LVDS pairs to CC. The other pair is currently unused.

A receiver will align itself with the transmitter at the beginning of every 32-bit word, using a start bit. While the receiver is receiving, its clock will deviate from the transmit clock. However, because the length of the transmitted word is short (32 bit), the clock does not deviate far enough to get out of sync with the transmit clock.

All packets over the backplane, moving in either direction (to and from CC), have the same format. A 2-byte preamble of 0xAAAA marks the start of a packet and is used to synchronize the receiver and the transmitter. A CRC checksum is used to check the integrity of the data.

The packet has a data portion that can be of variable length. For packets originating from the clock card (commands), the destination card is encoded in the packet. For reply packets originating on non-CC and transmitted over the point-to-point line, the packet-source is encoded in the packet.

There is no guarantee that a reply packet is generated for each command packet. No redundancy or retransmission is built in to the protocol. Instead, CC has an internal timeout mechanism to deal with cases that no reply was received.

The receiver ignores the packet if a valid preamble is not detected. A packet is pronounced invalid if the checksum is wrong, but a reply is sent back regardless.

3.3 Packet Structure and Content

A backplane packet is assembled as 32-bit words as shown in. In general, bit 0 of the 32-bit is transmitted first.

32-bit Word	Title	Description
0	Preamble	bit 31 to 16: 0xAAAA
	Command Type/Data Size	bit 15 to 12: unused bit 11: Command Type: Read=0 Write=1 bit 10 to 0: data size (number of 32-bit data words)
	Card Address	bit 31 to 24 (refer to [1])
	Parameter ID	bit 23 to 16 (refer to [1])
1	Status	bit 15 to 2 unused
		bit 1 command execution failed
		bit 0 CRC error for incoming command
2	Data 0	
3	Data 1	
…		
…	Data n-1	
2+n	Checksum	CRC checksum

Table 6 Packet over the MCE Backplane

Premable: The 16-bit preamble of 0xAAAA is used to mark the start of a packet.

Data Size: 11 bits are allocated to specify size of the payload in terms of 32-bit words (excluding card address/status/checksum words). Therefore, a BB packet may contain up to 2^{11}-1=2047 words of data. However, the largest BB packet is a quarter-frame of data (41×8×4=1312 words) transmitted from a single Readout Card (RC) to the Clock Card (CC).

Command Type: A single bit is used to encode command types with '1' indicating a write (or WB) command and '0' for a read (or RB) command. Refer to Figure 1, to see how other command types in the fibre packet are translated to one of the two when transmitted over the backplane. Note that

command type is also set for the reply packets where it refers to the command type of the command they are replying to.

Status: Currently only 2 bits are defined: bit 0 shows crc errors for the incoming command. Bit 1 shows that the command execution had failed.

3.4 Backplane-to-Fibre Packet Translation

The correlation between the Backplane packets and Fibre packets is shown in Figure 1:

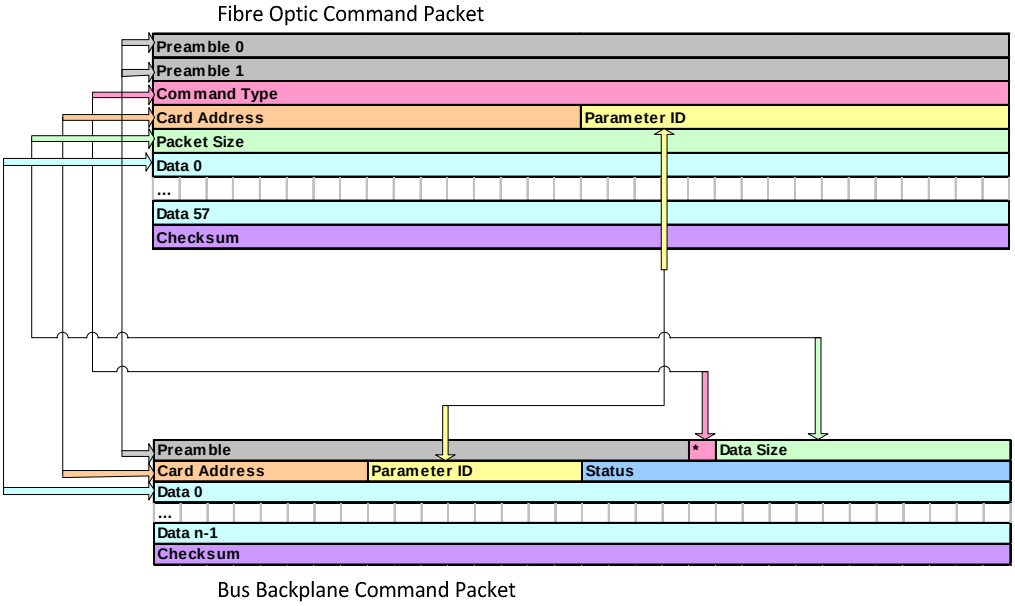

Figure 1 Comparing a Fibre packet to a Bus Backplane Packet

4. Clock-Card Communication with Power-Supply Card

4.1 Physical Layer

The Clock-Card and the Power-Supply Card (PSC) communicate via a 5-wire SPI interface. This interface consists of the following signals:

MOSI – Master Output - Serial output data from the PSC to CC
MISO – Master Input - Serial input to the PSC from CC
SCLK – Serial Clock - generated by PSC
SREQ – Service Request - generated by the CC
CCSS – Clock Card Slave Select - asserted by PS before SCLK for CC data transfers

4.2 Data Link Layer

All transfers are initiated by the CC via the "Service Request" Signal, SREQ. The PS card provides the SPI clock so it is the SPI "Master". This configuration was chosen as the controller on the PS card already communicates to other devices on the PS card as an SPI Master. The PS Card always has a 36-byte block of data, as defined in **Table 7** below, ready to transmit to the CC. To retrieve the data block the CC asserts SREQ. The PS responds with a 1.5MHz clock burst of 36×8=288 cycles (192µS transfer).
A checksum is included in the data block to detect bit errors in the data block. In the current implementation this is a simple checksum where error detection is sub-optimal as a trade-off for calculation speed. The checksum is calculated

Sum = 0 *(1 byte character)*
For each byte in Data Block (excluding ACK/NAK)
Sum = Sum + byte *(Ignoring overflow)*

Checkbyte = ~Sum +1 *(2's compliment)*

When Clock card receives the data block, it could check the following:
Checksum + (all other bytes in datablock) = 0. A non-zero value indicates an error.
But it does not currently.
As the data block is read by the CC on the MOSI line, a command, 2-byte long, is being sent to the PS card on the MISO line. To ensure the integrity of data, each command is sent 3 consecutive times. The PS card checks that at least 3 consecutive commands match then acts upon the command. If all commands match, the ACK character (0x60) is inserted in the data buffer otherwise the NAK character is inserted. The common periodic "Request Status" command is signalled by holding the MISO pin low for the whole 256 cycle clock burst.

4.3 Data Block

4.3.1 From PSUC to CC

Table 7 details the power-supply data block that is sent to CC.

Byte offset	Item	Number of bytes	Description
0	Silicon ID	4	32 least significant bits of the 48-bit Silicon ID
4	Software Version	1	Encoded as hex byte. 0xYZ = version Y.Z
5	Fan1 Tachometer	1	Currently not used
6	Fan2 Tachometer	1	Currently not used
7	PSUC Temperature	1	8 bit two's compliment (1 deg. increments)
8	PSU Temperature	1	8 bit two's compliment (1 deg. increments)
9	Heat Sink Temperature	1	8 bit two's compliment (1 deg. increments)
10	ADC Offset	2	Digitized Ground (bipolar, 2 bits/deg C)
12	Supply Voltage 1	2	+Vcore Supply – unipolar scaled to 73.2%
14	Supply Voltage 2	2	+Vlvd Supply – unipolar scaled to 73.2%
16	Supply Voltage 3	2	+Vah Supply – unipolar scaled to 73.2%
18	Supply Voltage 4	2	+Va Supply – unipolar scaled to 73.2%
20	Supply Voltage 5	2	-Va Supply – unipolar scaled to 73.2%
22	Supply Current 1	2	Current +Vcore– unipolar scaled to 61%
24	Supply Current 2	2	Current +Vlvd– unipolar scaled to 61%
26	Supply Current 3	2	Current +Vah– unipolar scaled to 61%
28	Supply Current 4	2	Current +Va– unipolar scaled to 61%
30	Supply Current 5	2	Current -Va– unipolar scaled to 61%
32	Status Word	2	For future expansion (Not defined yet!)
34	ACK/NAK	1	ACK if command correct/NAK otherwise
35	Checksum (Check Digit)	1	2's complement of Running sum of byte 0 to 33 excluding ACK/NAK
	Total	36	36×8 = 288 clocks on the SPI Interface

Table 7 Power-Supply Controller Data Block*

Note *: For debugging purposes, in cases that clock-card communication is down, this data block can also be read through an RS232 serial-port connector on the front-panel of the MCE. The RS232

settings are: 9600 baudrate, 8 data-bit, no parity, 1stop bit, no flow control. For more details and list of available commands refer to **Error! Reference source not found.**.

4.3.2 From CC to PSUC

Table 8 lists the commands that can be passed to the PSUC card. Commands are encoded as 2-Bytes (ASCII).

Command Title	Command Code
Request Status	0x0000
Cycle Power	0x4350 (“CP”)
Reset MCE (assert BRST)	0x524D (“RM”)
Turn Off	0x544F (“TO”)

Table 8 Command Encoding for Power-Supply Card to Clock-Card Communication

CC sends commands to the PSUC as the PSUC data block is received. As each data block is 36 Bytes and each command is 2 Bytes, a command may be repeated up to 18 times during that period. Holding the MISO pin low for the whole 256-cycle clock burst indicates the common periodic “Request Status” command. This is essentially the default command.

5. MCE / Sync Box Communication

5.1 Physical Layer

A fibre-optic link is used to communicate between the MCE and an external synchronization source.

5.2 Data-Link Layer

6. Future improvements (optional)

7. Glossary

CC Clock Card

PSUC Power Supply Unit Controller

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8. References

[1] “Clock Card Description”, SC2_ELE_S580_501, www.phas.ubc.ca/~mce/mcedocs
[2] “ARC64 250 MHz PCI Interface Board User’s Manual”, *Astro-Cam lab at San-Diego State University*, http://www.astro-cam.com/
[3] “SCUBA-2 Data Acquisition Software Overview – Part two Protocols”, SC2/SOF/S200/014, *UK Astronomy Technology Centre*.
[4] “MCE Command Description”, SC2_ELE_S580_515
[5] “Common Features for all MCE Cards”, SC2_ELE_S580_527, *University of British Columbia*
[6] “Firmware Overview”, SC2_ELE_S500_23, Version 2, *UK Astronomy Technology Centre*

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