

## Readout Card Pre-Amplifier settling time tests

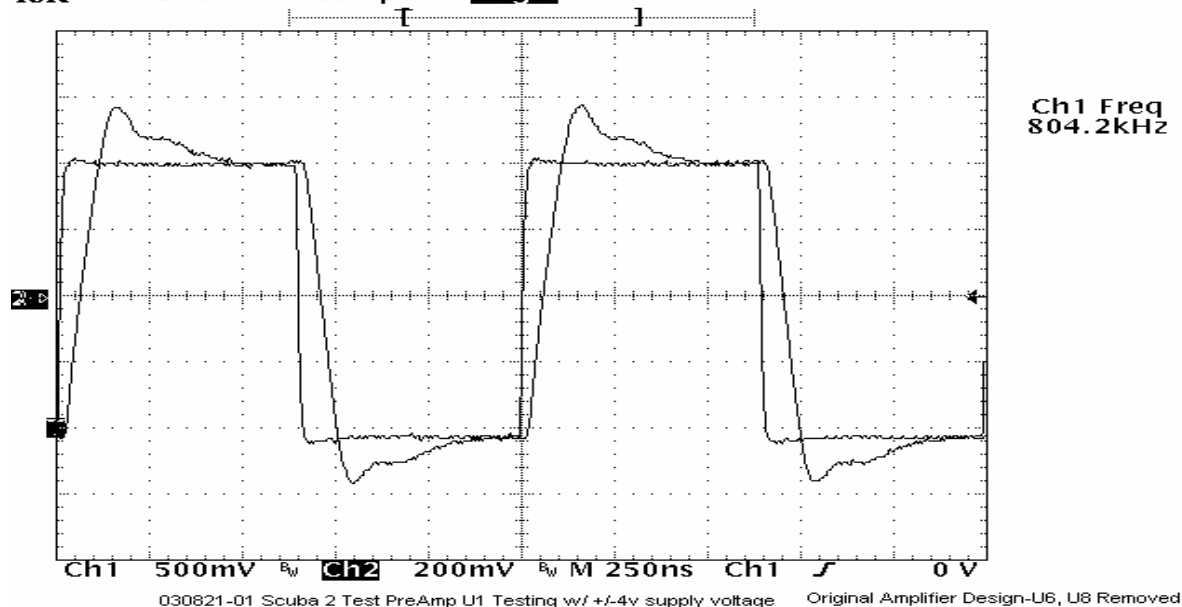
### Introduction

This document compiles the results of testing the Readout Card Pre-Amplifier Circuitry. The main purpose was to verify the fastest settling time for the Linear Technologies Operation Amplifier (Op-Amp), LT1028. Also tested were the LT1128, and the Analog Devices Op-Amp, AD797.

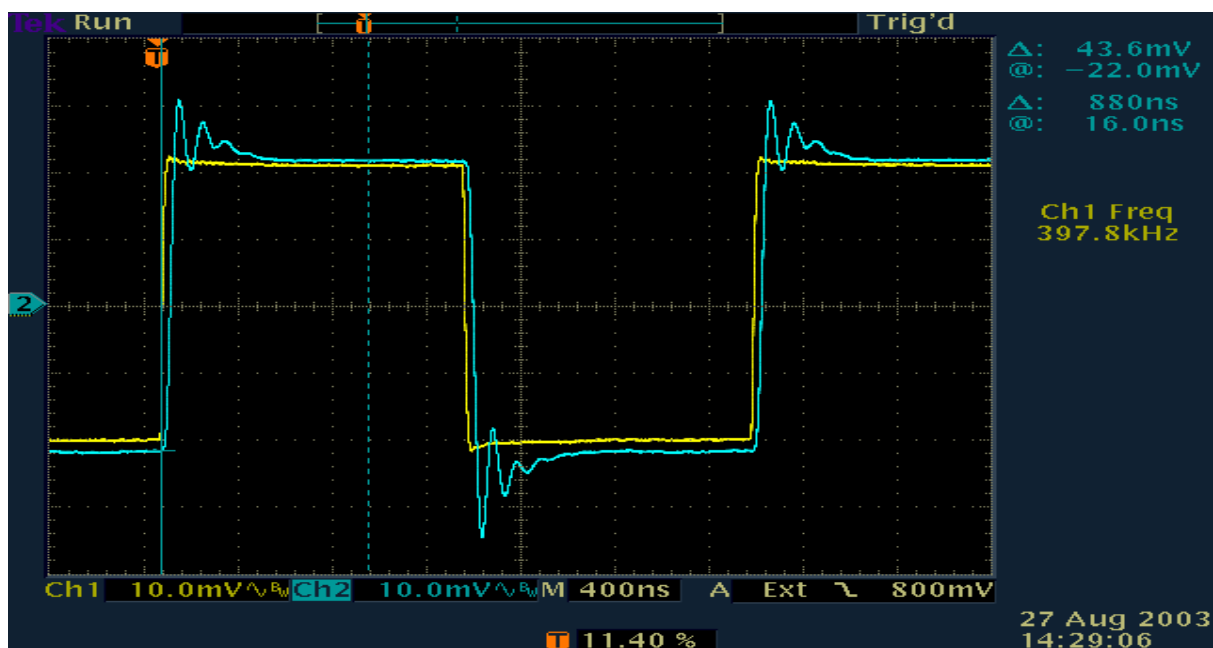
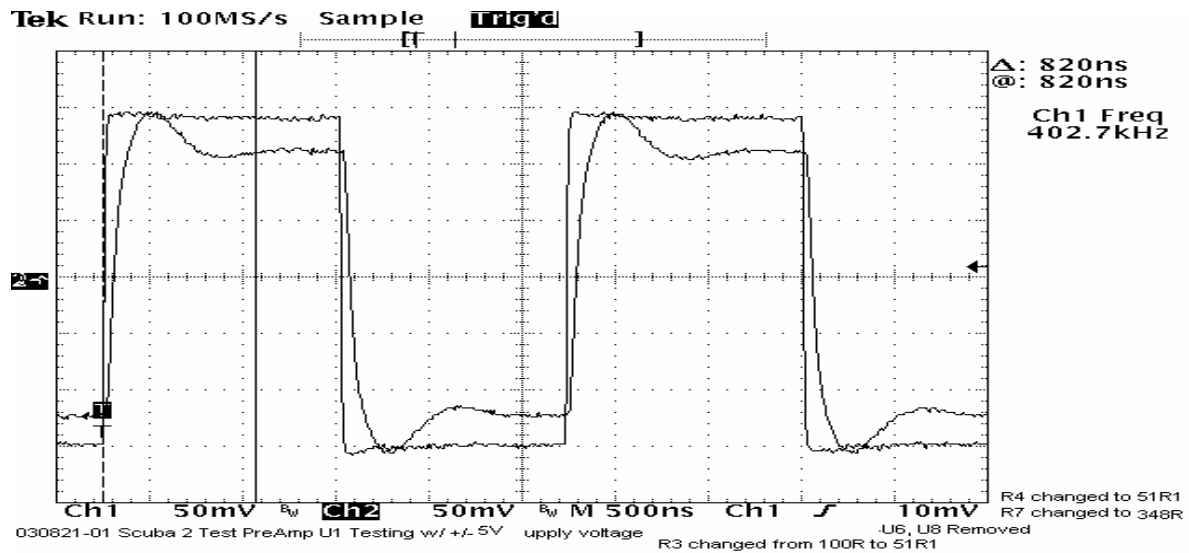
### First Stage Testing

For initial testing I used original schematic design for testing. Initial tests showed the LT1028 settling time was not suitable for our application. A typical settling time from 700 to 900ns was observed

**Tek Run: 200MS/s Sample** **Trig**



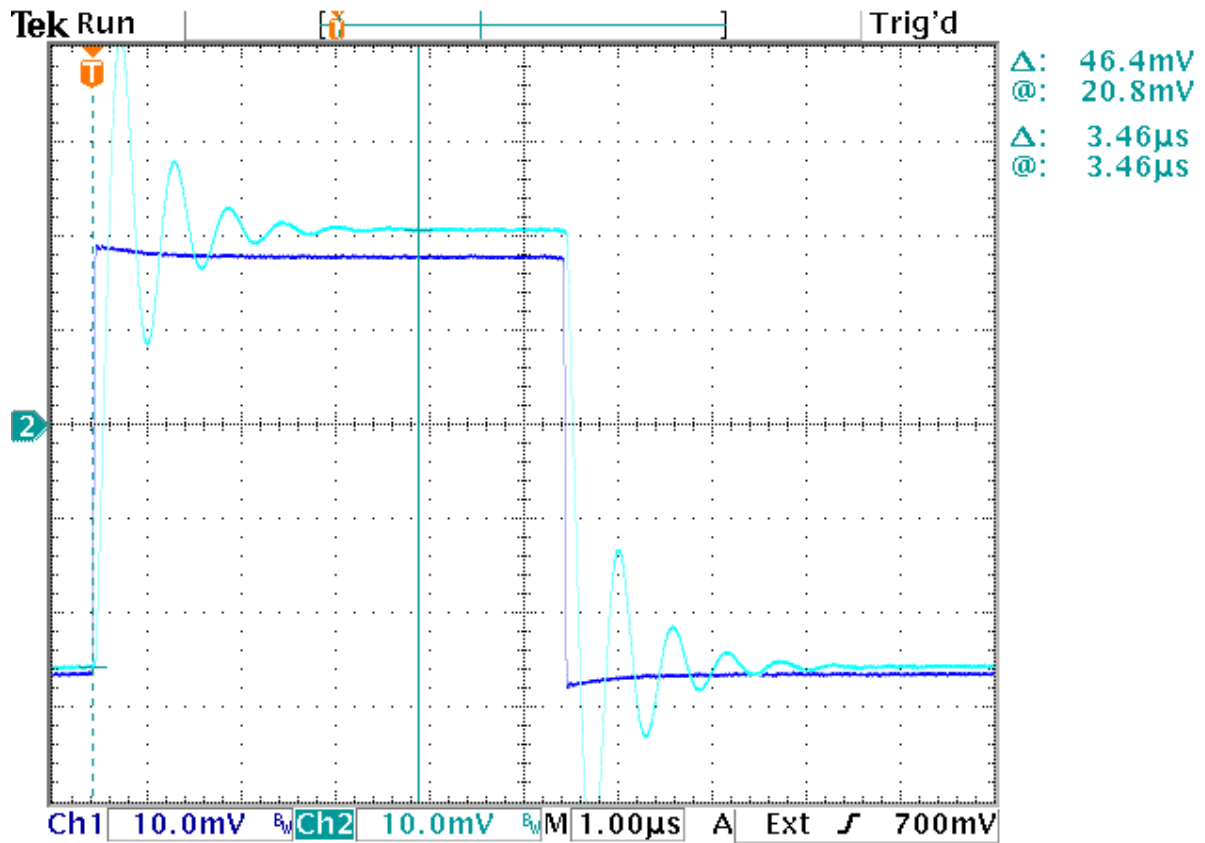
I changed the gain resistor values to check for differences in settling time. By removing the voltage regulators (U6 & U8) it allowed adjusting the voltage supply level to op-amp. Stan and I were interested to whether or not the voltage level impacted the performance of the op-amp. We did not observe any significant differences, if any at all, in performance with voltage supply level. We used min/max supply levels of +/-4.5V, +/-5V, and +/-12V for testing.



Gain = 4  
 +/-12V Supply Voltage  
 R3 = 51R1  
 R7 = 300R  
 R4 = 100R

## First Stage Testing – LT1128

According to the LT1028/LT1128 data sheets, the LT1128 is better suited for non-inverting applications. I briefly tested the an LT1128 for the first stage. The below picture does not show impressive results. I did not investigate further time on improving the performance of the LT1128. This measurement was taken at the output of the second stage.



9 Sep 2003  
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First Stage: U1 = LT1128  
Gain = 2

R3 = 51R1  
R4 = 20R  
R7 = 20R

Second Stage: U2 = AD797  
Gain = 4

R13 = 300R  
R10 = 100R  
R12 = not populated

## First Stage Testing – AD797

Further first stage testing with the AD797. Several gain resistor values were used in the testing. For brevity, only one of the combinations is posted below. The best settling time achieved from the AD797 was 220ns, far better than the LT1028 and LT1128.

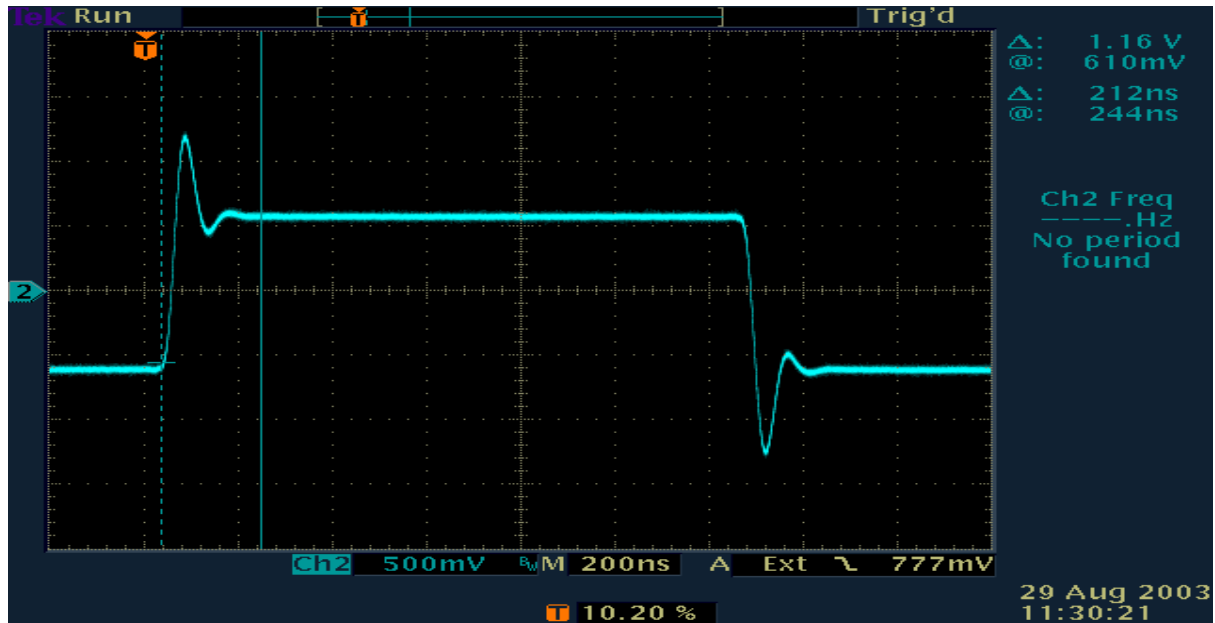


R7 = 150R  
R4 = 51R1

Peaking Frequency: 9.0MHz  
90° Phase shift, input to output 17.8 MHz

## Third Stage Testing

Continuing the tests with AD797 in the first & second stage, the third stage was populated as per schematic design. Measurement captured at output of third stage.



First & Second Stages

Gain = 4

+/-5V Voltage Supply f = 800 KHz

R3 = 51R1  
R7 = 150R  
R4 = 51R1

Third Stage:

Gain = 6

R16 = 200R

R17 = 1K00

Peaking Frequency: 10.0MHz  
90° Phase shift, input to output 17.8 MHz

## Fourth Stage Testing

The following pictures show the output of the fourth stage. The first two pictures show the settling times and latter two shows the group delay from input to stage one to output of fourth stage.

First Stage:

U1 = AD797

Gain = 4

R3 = 51R1

R7 = 150R

R4 = 51R1

Second Stage:

U2 = AD797

Gain = 4

R10 = 51R1

R13 = 150R

R12 = not populated

Third Stage:

U3 = AD848

Gain = 6

R16 = 200R

R17 = 1K00

Fourth Stage:

U4 = AD8138

Gain = 2

R18, R19 = 237R

R20, R21 = 475R

R22, R23 = 24R3

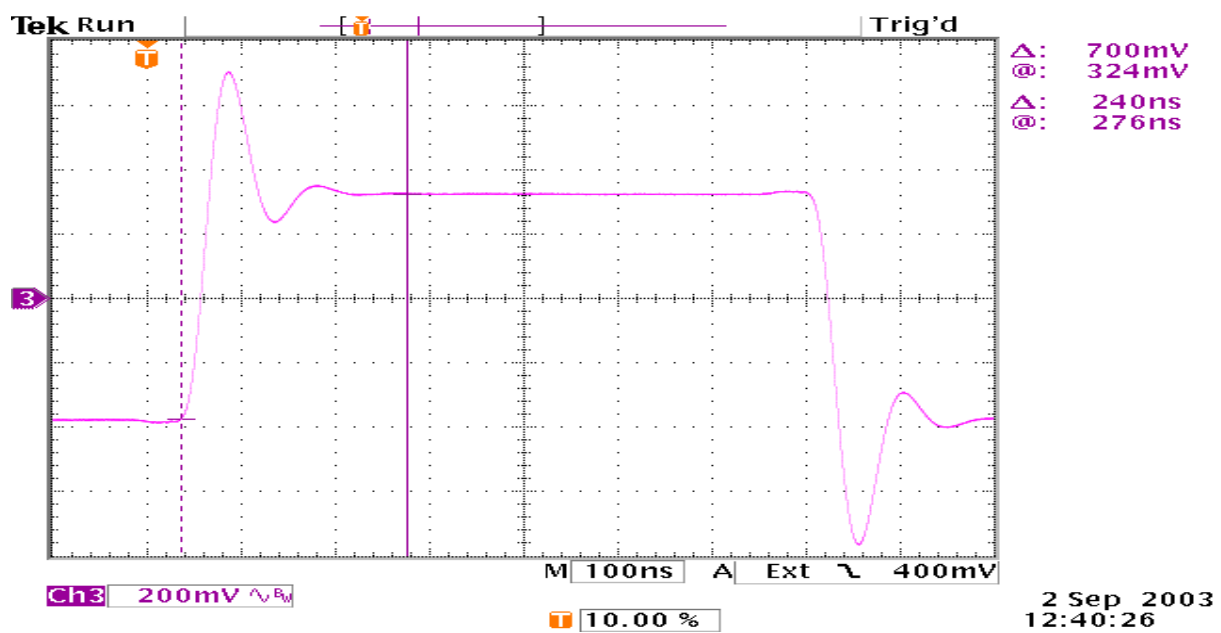
Single-ended Gain ~ +100 & -100

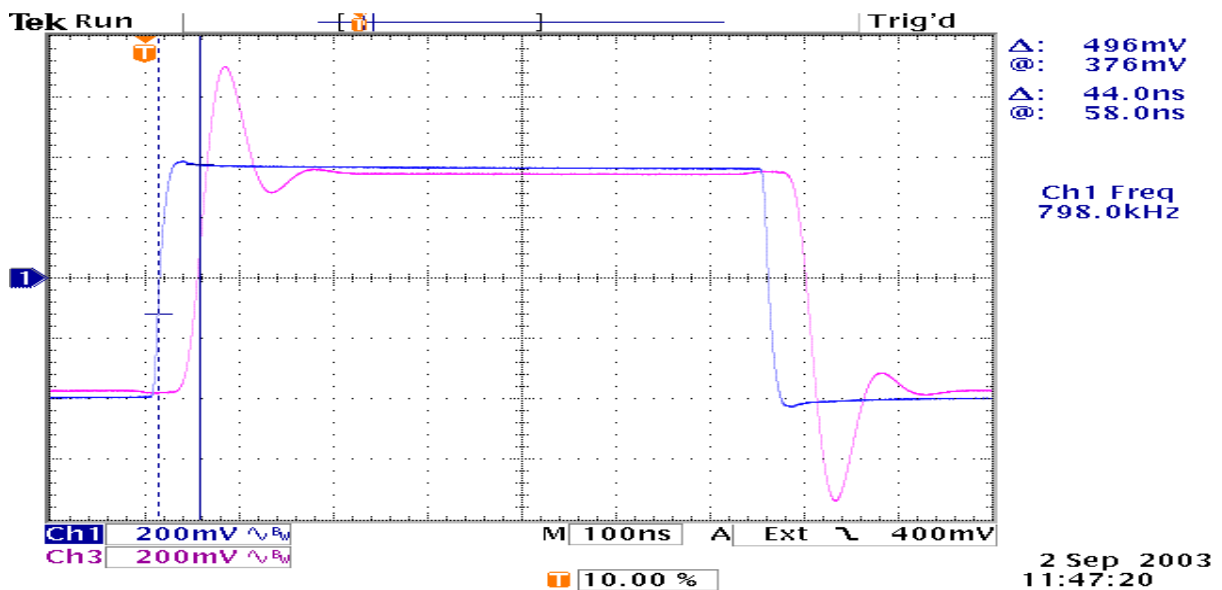
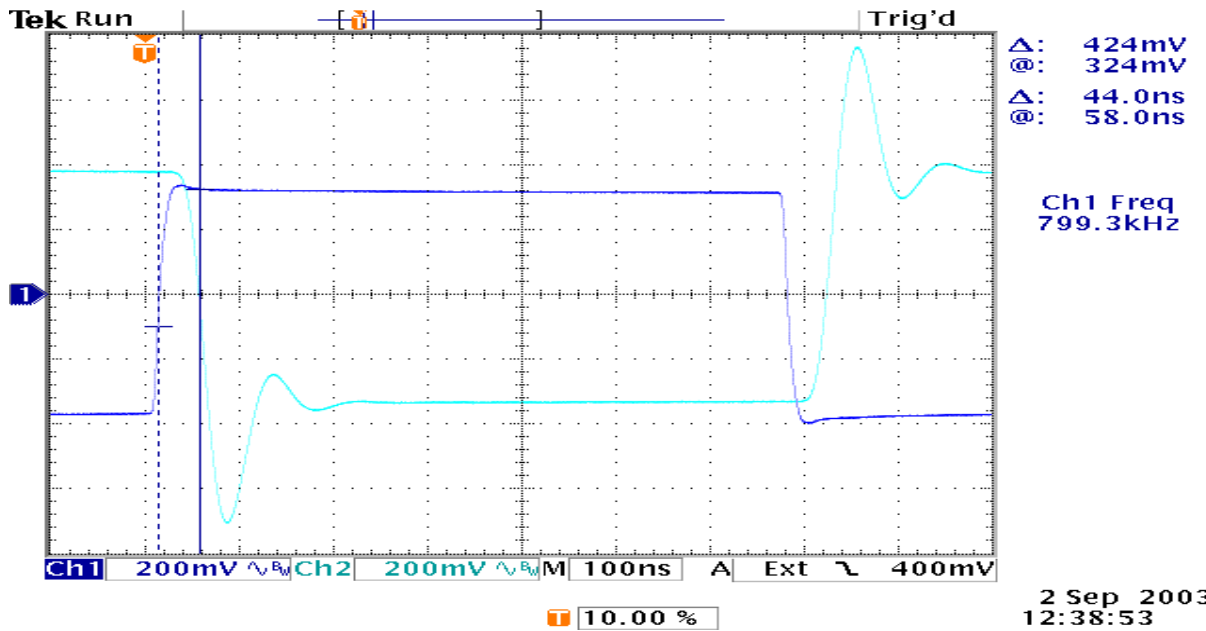
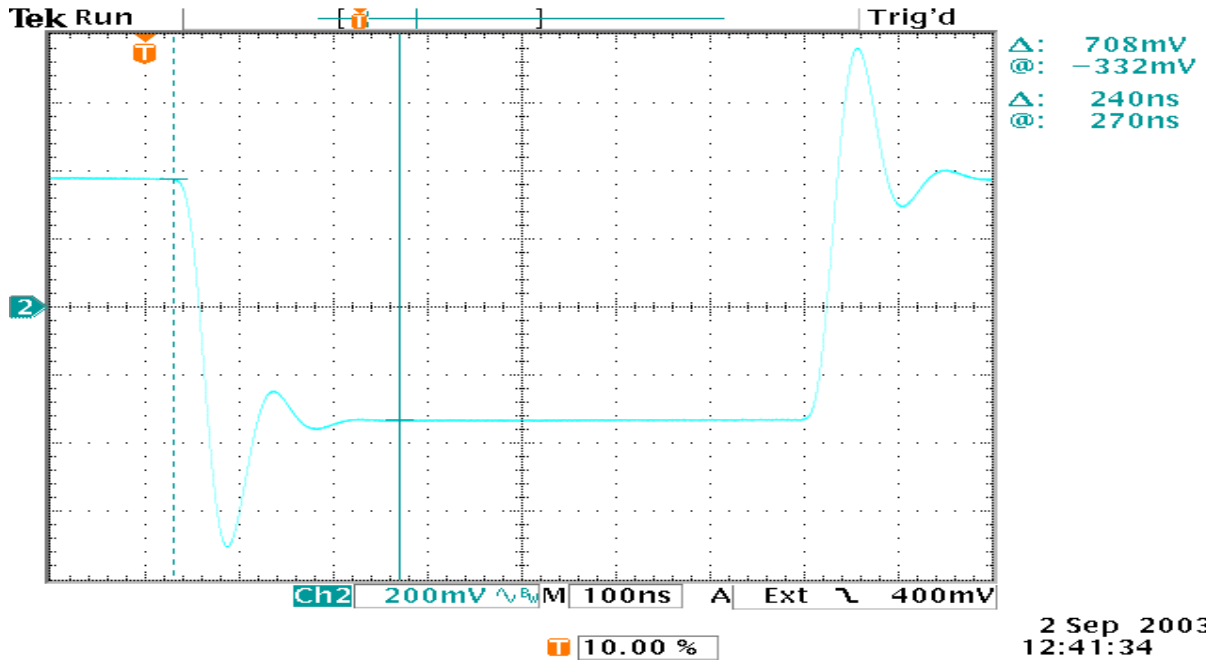
Differential Gain ~ +200

U13 AD6644AST not installed

U4 Pin2 VREF\_ADC connected to VRef ~ 2.50VDC

Power regulation installed as per schematic.





## **Appendix**

### ***Equipment Used:***

Tektronix TD 3020 Oscilloscope w/ Tek 6130 10Mohm 10x probes

Tektronix TD 3054B Oscilloscope w/ Tek 6139A 10Mohm 10x probes

Tektronix FG504 40MHz Signal Generator

Agilent 33120A 15MHz Signal Generator