SCUBA-2 Address Card DAC Bus Scheme

1. Summary

The purpose of this document is to analyze the requirements for the DAC row-addressing buses on the Address Card (AC), and give recommendations for how many DACs should be multi-tapped from each bus, and what width each bus should have.

2. References

[1] Analog Devices 14-Bit, 165 MSPS TxDAC® D/A Converter 9744 Data Sheet
[2] Stratix Device Handbook, Using Selectable I/O Standards in Stratix & Stratix GX Devices chapter
[3] Minimizing Ground Bounce & VCC Sag, Altera White Paper

3. Introduction

Each subrack has one Address Card (AC). The AC will activate one row of SQUIDS on the SCUBA-2 subarray at a time. There are 41 rows per sub-array, so the AC will push 41 currents into the subarray at once. On the AC, each current will be generated by a 14-bit 165 MSPS AD9744 DAC.
To select a row, the AC will do the following:
(a) Apply 'off' currents to all rows that will be de-selected ('off' currents may differ from row to row).
(b) Apply an appropriate biasing current to the row that is to be selected (row-to-row selection currents may differ).

Several options exist for how to control the DACs. Discussion has centred on how many data bits each DAC should use and how many buses should be used to control the 41 DACs. Currently, in NIST's design, each DAC has its own data bus and each bus is 14 bits wide. In UBC's present design, each DAC has its own bus, and each bus is 8 bits wide.

4. Analysis

4.1 Requirements

There are some requirements to bear in mind while analyzing the AC bus configuration problem:
(a) The FPGA package that will be used must have enough user-I/O to support the addressing scheme that will be chosen.
(b) To help in debugging, all bus lines will be routed on the same PCB layer, side-by-side. This will require a large enough gap between DACs to route a whole number of buses on a single layer.
(c) A cap on the total FPGA I/O usage of 80% is recommended to facilitate synthesis and PCB-routing, and for contingency.
(d) To help reduce the number of possible firmware bugs, the bus scheme should be as modular as possible. For example, each bus should have an identical number of DACs multi-tapped from it.

4.2 Decision Factors

To determine the appropriate bus width and DAC:bus ratio, the following considerations are made:

(a) FPGA I/O availability

To ease constraints on synthesis and PCB routing, and to provide some contingency, it will be reasonable to require a total I/O usage cap of 80% on any given package. At last count, there were 48 I/O pins reserved for essential functionality on the AC. This number did not include the pins for DAC data buses and clocks.

To determine whether a certain FPGA package has enough I/O to support a particular bus scheme, the following relation will be used:

$$\frac{[48\,\mathrm{Re}\,servedIO]+[DACIO]}{0.80} \le UserIO$$

Where 'DACIO' is the number of I/O pins required for a particular bus configuration, and 'UserIO' is the maximum number of user I/O pins available in a certain package, as listed in the table below:

Family Member	User I/O	DAC I/O
EP1S10	426	293
EP1S20	586	421
EP1S25	597	430
EP1S30	589	423
EP1S40	615	444

Figure 1. Maximum Number of User I/O Pins Available in the 780-Pin FineLine BGA 29x29 mm, and Number of I/O available for DAC Buses

Ideally, one would like each DAC to have its own full-resolution bus. However, if 41 14-bit buses were used on the AC, 615 DAC I/O (including clock signals) would be required. According to the relation above, a package with 886 user I/O would be necessary for such a scheme. A 886-pin package does not exist, and the closest to it (the EP1S40) has a mere 615 user I/O. Therefore, a balance must be reached between the number of I/O used, and the extensiveness of the bus configuration. The firmware requirements of the AC will be less then on any other card, so some effort may be made to use the smallest family member of the 780-pin class of FPGAs (i.e. the EP1S10).

The table below shows the number of I/O pins that would be necessary for several different bus schemes. Note that the '# Buses' column figures include a bus for the dark row DAC. It is assumed that the dark-row DAC will not share its bus with any other DACs. The numbers in the '# Buses' column have been conjured so that the number of multi-tapped DACs per bus is a multiple 40. This will ensure that an equal number of multi-tapped DACs hang from each bus, and will help to reduce the number of possible firmware bugs. The 'DAC I/O Required' column includes I/O used for the dark-row DAC. It will be important to compare this column to the 'DAC I/O' column in Figure 1. The yellow row in Figure 2 represents the most I/O-intensive bus configuration which can be used with the EP1S10, which from the table above has 292 I/O available for DACs. The blue row represents the most I/O-intensive bus configuration which can be used with all the other devices (EP1S20, EP1S25, EP1S30, EP1S40). No 780-pin BGAs can support a scheme more intensive than in the blue row.

It is also worth noting that the most intensive bus scheme to fit on all FPGAs and offer full 14-bit bus-resolution is outlined in green.

# Buses	#DACs/Bus	# Bits/Bus	DAC I/O Required
3	20	8	27
3	20	10	33
3	20	12	39
3	20	14	45
5	10	8	45
5	10	10	55
5	10	12	65
5	10	14	75
6	8	8	54
6	8	10	66
6	8	12	78
6	8	14	90
9	5	8	81
9	5	10	99
9	5	12	117
9	5	14	135
11	4	8	99
11	4	10	121
11	4	12	143
11	4	14	165
21	2	8	189
21	2	10	231
21	2	12	273
21	2	14	315
41	1	8	369
41	1	10	451
41	1	12	533
41	1	14	615

Figure 2. Several Different DAC Bus Configurations, and Their I/O Requirements

(b) Ground Bounce or V_{CC} Sag

Switching noise can occur in the form of either 'Ground Bounce' or 'V_{CC} Sag'. For a thorough discussion on these see [3]. Switching noise is considered here because measures taken to reduce it will have implications on the number of I/O that will be available for a DAC bus scheme.

Loosely speaking, switching noise occurs in the following manner: every time that a voltage level changes on a bus line or clock line, some voltage noise is produced which obeys the relation below:

$$V = L\frac{dI}{dt}$$

The differential term in this equation corresponds to the I/O current's rate-of-change during an edge transition. The rate-of-change depends on the slew rate of the FPGA I/O pins as well as the number of DACs that are multi-tapped from a bus. The total voltage noise produced depends on both these factors, as well as the inductance in the FPGA pins, device packaging and connections to the board ground.

Some design methods can reduce the inductance, reduce the rate of change of current or decrease the amount of ground bounce and V_{CC} sag. These design methods include the use of:

(a) Flip Chip device packages
(b) Slow slew rate
(c) Limit the number of simultaneously switching output (SSOs) per I/O bank
(d) Spread out SSOs
(e) Programmable GND and V_{CC} pins
(f) Out-of-phase simultaneously switching output (SSOs) using phase-locked loops (PLLs)
(g) Out-of-phase simultaneously switching output (SSOs) using programmable output delay option
(h) Series termination resistors

(i) Series-RC parallel terminations
(j) Decoupling capacitors

Only (c), (d) and (e) have implications in regards to the bus configuration scheme, but can contribute significantly to reducing bounce and sag, as seen in the table below.

Design Method (APEX EP20K100EFC324-1X)	% Improvement	
	GND Bounce	V_{CC} Sag
Device package (Flip Chip vs. wire-bonded)	72	58
Slow slew rate	65	61
Half the number of SSOs	11 to 35	12 to 31
Tri-state every other I/O pin (- Z - I/O- Z - I/O - Z-)	13	28
Tri-state every third I/O pin (- Z - I/O - I/O - Z - I/O - I/O - Z-)	7	25
Programmable GND or V_{CC} on every other I/O pin. Programmable GNDs and V_{CC} s are connected to board GND or V_{CC} (- V_{CC} - I/O - GND - I/O - V_{CC} -)	45	49
Programmable GND or V_{CC} on every other I/O pin. Programmable GNDs and V_{CC} s are not connected to board GND or V_{CC} and have a 7.5-pF load.	24	22
Programmable GND or V_{CC} on every 3rd I/O pin. Programmable GNDs and V_{CC} s are connected to board GND or V_{CC} (- V_{CC} - I/O - I/O - GND - I/O - I/O - V_{CC} -)	41	22
Programmable GND or V_{CC} on every third I/O pin. Programmable GNDs and V_{CC} s are not connected to board GND or V_{CC} and have a 7.5-pF load.	71	25
Programmable GND or V_{CC} on every third I/O pin with a 10-Ω series resistor on each I/O pin. Programmable GNDs and V_{CC} s are not connected to board GND or V_{CC} and have a 7.5-pF load.	68	31
PLL clock drives every other I/O pin (clock shift of 341 ps)	12	24
Programmable output delay (t_{co} 520 ps different)	12	25
10-Ω series termination resistor (interpolated)	46	12
Series-RC parallel termination (100 pF and 50 Ω)	47	31

Figure 3. Design Methods to Improve GND Bounce and V_{CC} Sag

(c) Addressing Speed

Complete array data are available at a rate of approximately 20 kHz, or every 50µs. This means that each of the 41 row-addressing DACs will be switched on and off in sequence during one 50µs period. 50µs divided into 41 slices corresponds to 1.220µs of dwell time per row. At the beginning of a dwell time, the last row's DAC will have its 'off' value clocked in, the present row's DAC will have it's 'on' value clocked in, and some time will be allocated for the DACs to settle. The settling time is about 360ns, leaving 860ns for sampling the SQUIDs at 50MHz from the Readout Cards. In one 860ns period, and RC can record about 42 samples. There are relatively few samples per frame, so care must be taken so as not to decrease this number further. To address this concern, the AC buses will provide means to clock in both the 'on' and 'off' values in parallel. In the prototype MUX at NIST, DACs switch simultaneously. NIST has said that simultaneous selection/deselection of two rows does not have a dominant effect on the system settling time. Simultaneous selection/deselection imposes the use of at least two interleaved data buses on the AC.

The internal frequency of the AC FPGA will be 400 MHz (16 x 25MHz reference clock). Two clock cycles will be necessary to clock a value into a DAC – one to assert a value on the data bus and let the value settle, and another to latch in that value for a specified time. Two 400 MHz cycles correspond to 5ns or ¼ of a 50Mhz sampling period. Thus loading two values simultaneously may allow the RC to actually take 42 readings.

For reference, an AD9744 will require an Input Setup Time (t_S) of 2.0 ns, followed by an Input Hold Time (t_H) of 1.5 ns, and a Latch Pulsewidth (t_{LPW}) of 1.5 ns (see the figure below).

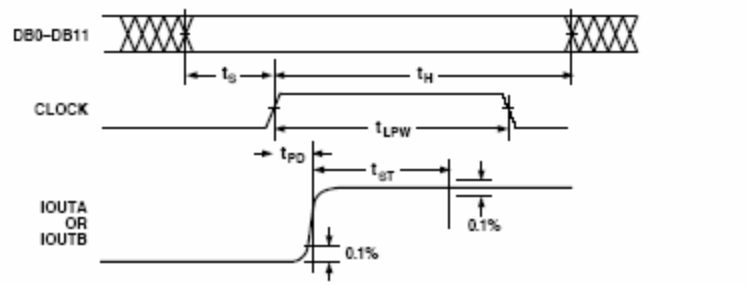

Figure 4. AD9744Timing Diagram

(d) Bit resolution, using 14-bit DACs

UBC will use the AD9744 DAC for row-addressing. This DAC is capable of current output between 2-20mA. This output current is converted to a voltage between 0.1-1.0V using a shunt resistor to ground ('R2' in the Figure below). This voltage is RC-filtered using 'R3' and 'C8', and then converted by 'RL' (see Figure 1) into a current which is fed to a row of first-stage SQUIDs in a sub-array. 'RL' will be approximately 5.1kΩ, which means that the full-scale current flowing into the first-stage SQUIDS will be about 196μA. During meetings in December 2002, NIST stated that 1-2μA variations in SQUID bias don't affect noise. This means that about 196 DAC-values, or 8-bits of resolution (256 values) should be sufficient to adequately specify first-stage SQUID biases.

As a result of this, in UBC's current design the 6 LSBs on the AC DACs have been gounded, and the 8 MSBs are used for specifying bias currents. However, the schematic design and PCB layout is not appreciably extended if each bus is widened to a full 14 bits. If this is done then a further 6 bits of biasing resolution will be available. However, if it is found that this resolution is not useful, this lines can be directly grounded through the FPGA to the ground plane, and will not contribute to the noise on the AC. In fact, this may help reduce bounce and sag.

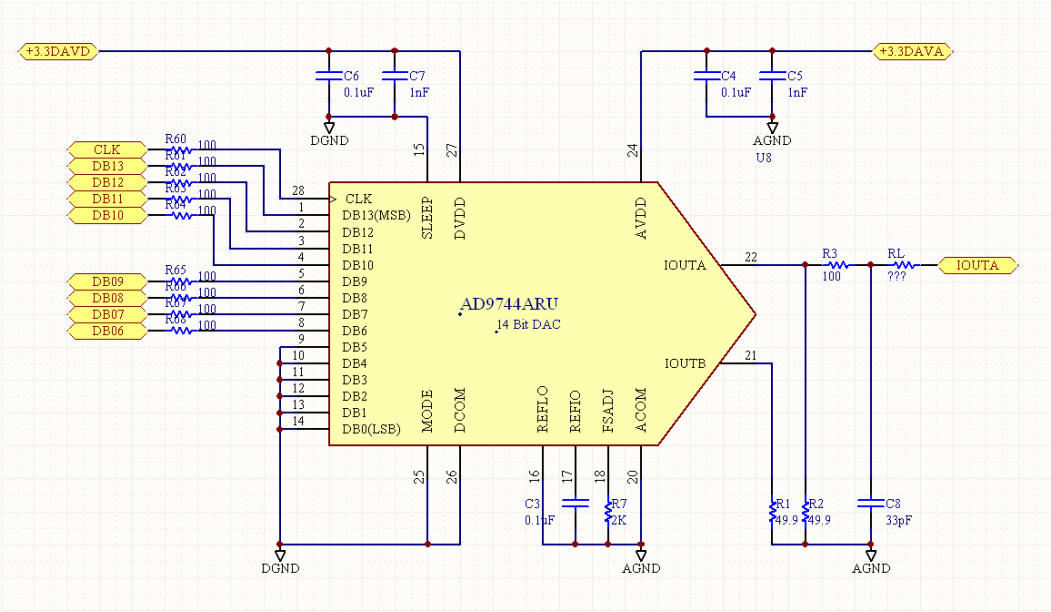

Figure 5. Current AC DAC Design

Pin No.	Mnemonic	Description
1	DB13	Most Significant Data Bit (MSB)
2–13	DB12–DB1	Data Bits 12-1
14	DB0	Least Significant Data Bit (LSB)
15	SLEEP	Power-Down Control Input. Active high. Contains active pull-down circuit; it may be left unterminated if not used.
16	REFLO	Reference Ground when internal 1.2 V reference used. Connect to AVDD to disable internal reference.
17	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled (i.e., tie REFLO to AVDD). Serves as 1.2 V reference output when internal reference activated (i.e., tie REFLO to AGND). Requires 0.1 µF capacitor to AGND when internal reference activated.
18	FS ADJ	Full-Scale Current Output Adjust
19	NC	No Internal Connection
20	ACOM	Analog Common
21	IOUTB	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
22	IOUTA	DAC Current Output. Full-scale current when all data bits are 1s.
23	RESERVED	Reserved. Do Not Connect to Common or Supply.
24	AVDD	Analog Supply Voltage (3.3 V)
25	MODE	Selects Input Data Format. Connect to DGND for straight binary, DVDD for two's complement
26	DCOM	Digital Common
27	DVDD	Digital Supply Voltage (3.3 V)
28	CLOCK	Clock Input. Data latched on positive edge of clock.

Figure 6. AD9744 Pinout

(e) FPGA I/O Driving Capabilities

The AD9744 Digital Specifications [1] state that both input logic "1" and "0" currents range from –10 to +10 µA. The limitations on total current draw from 10 consecutive I/O pins (including two dual purpose pins for external reference resistors within these 10 I/O pins) should not exceed 200 mA for thermally-enhanced cavity down packages or 150 mA for non-thermally enhanced cavity up and non-thermally enhanced FineLine BGA packages[2]. Even if there was only one data bus to all DACs, the maximum current across 10 pins would be

$$[41 inputs] * \left[10 \frac{\mu A}{input}\right] * [10 pins] = 4.1 mA$$

4.1 mA distributed across ten pins is well within specifications. This means that line drivers will not be necessary, regardless of how many DAC inputs are driven by each FPGA I/O pin.

(k) Addressing Sequence

In a multi-tapped bus configuration scheme where two DACs need to change values at the same time, some restrictions are placed on the sequence in which rows may be addressed. For example, suppose the AC has two buses that each serve 20 DACs. Then each address change will require the simultaneous use of both buses (one to deselect the active row, and the other to select the next row). This means that the AC will be limited to selecting 1 of 20 DACs that are multi-tapped from the bus that is not used to deselect the previously active row. The table below lists a few possible bus configuration schemes, and for each the number of DACs that will be available for addressing while one bus is used to deselect the previously active row. Clearly, the more buses there will be, the more DACs will be available for addressing. Note that the '# Buses' column figures include a single bus for the dark row DAC. It is assumed that the dark-row DAC will not share a bus with any other DACs, but will have its own. All other DACs will be split equally between the remaining buses.

# Buses	#DACs Selectable
3	21
5	31
6	33
9	36
11	37
21	39
41	40

Figure 7. Number of DACs That Are Selectable While One Is Being Deselected

(l) PCB Line Failure

If a DAC data-bus line fails during testing or during operation, it may be possible to continue normal observation until it is convinient replace the AC. Decisions to continue observing will depend on the significance the bus-line that failed, but may also depend on the number of DACs affected by the failure. Clearly, if there are more buses, then fewer DACs will be affected by a individual bus failure.

#Buses	#DACs Affected by Bus Failure
3	20
5	10
6	8
9	5
11	4
21	2
41	1

Figure 8. Number of DACs affected by the Failure of One Bus

(f) PCB routing

Using components in the AC design, an experimental PCB layout was done on a 220mm deep card. It was found that each DAC (with supporting circuitry) required 13mm^2 on both sides of the board for surface mount components. When all 41 DACs were placed on a grid pattern on the AC, it was found that a 7x6 (rows x columns) or 8x5 array fit best on the board. A 6x7 configuration began to encroach on the digital portion of the AC, which will sit near the BB connector. The 7x6 configuration (see Figure 9, below) fit well in the analog portion of the AC (near the IB connector), while allowing sufficient space between the rows of DACs to route the widest (14-bit) buses. The 8x5 configuration (see Figure 10) began to encroach on the top and bottom extremities of the card, which meant that the rows of DACs would have to be closer together, thus reducing the maximum bus-width per layer to 10 bits.

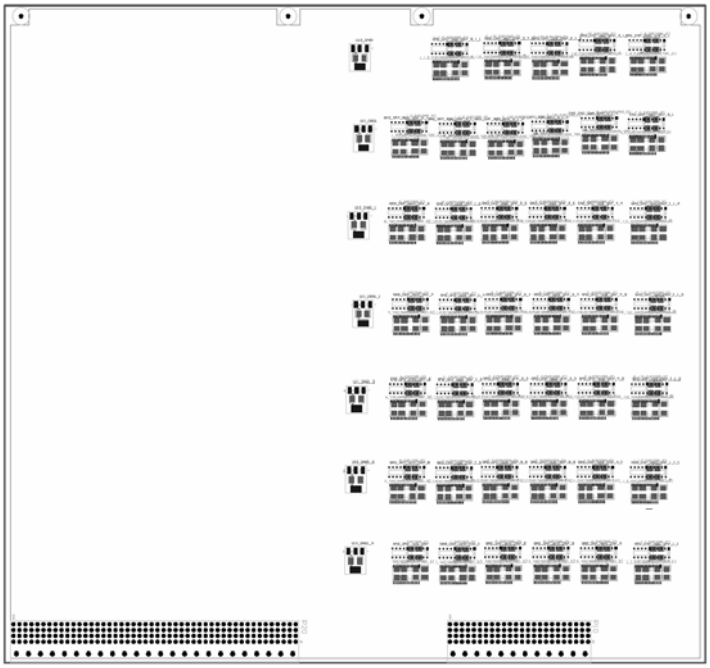

Figure 9. 7x6 DAC PBC Layout

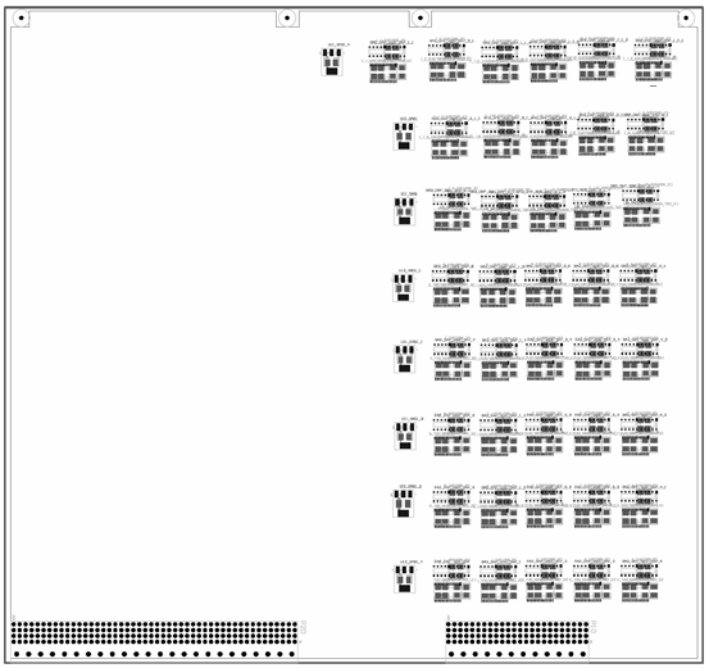

Figure 10. 8x5 DAC PCB Layout

Some calculations concerning the viability of these PCB configurations are summarized in the following table below. Note that the table assumes 41 data buses are used – one for each DAC.

DAC Layout Configuration	7x6	7x6	8x5	8x5	8x5	
Parameters						**Units**
Average Trace Width	0.2032	0.2032	0.2032	0.2032	0.2032	mm
Average Trace Spacing	0.2032	0.2032	0.2032	0.2032	0.2032	mm
Board Depth	220	220	220	220	220	mm
Unusable Board Space	8	8	8	8	8	mm Faceplate
	25	25	25	25	25	mm IB Connector
DAC ICs Width	13	13	13	13	13	mm
DAC ICs Length	13	13	13	13	13	mm
Bus Docking Space	4	4	4	4	4	mm
DAC Regulator Width	10	10	10	10	10	mm
DAC Regulator Length	10	10	10	10	10	mm
# DACs Per Regulator	6	6	6	6	6	DACs/Reg
# DACs	40	40	40	40	40	DACs
# Dark DACs	1	1	1	1	1	DACs
# DAC Columns (inc dark DAC)	7	7	8	8	8	DACs
DAC Bus Data Width	14	8	14	12	10	bits
Calculations						
# DACs Per Column	6	6	4	4	4	DACs
DAC Bus Width	5.6896	3.2512	5.6896	4.8768	4.064	mm
Minimum Spacing Req'd by DAC Column	17	17	17	17	17	mm
Total Width Required by DAC Columns	136	136	153	153	153	mm
Residual Width for Bus Routing	51	51	34	34	34	mm
# Buses Per Layer	1.280531898	2.24093082	0.74697694	0.871473097	1.045767717	Bus/Layer
# Layers Req'd for 41 Buses	6	3	∞	∞	4	Layers

Figure 11. Two DAC PCB-layout Configurations, With Different-Sized Buses

Note that none of these schemes require more layers than are reasonable for the AC. It is thought that the AC will have 6-8 layers. The most intensive scheme listed above will route 41 14-bit buses in a 7x6 format and will require 6 layers to fit the buses between the DACs. Note that if DACs will be placed in a 8x5 format, there won't be enough room between DACs to route 14- or 12-bit wide buses on the same layer. This would violate one of the requirements in §4.1. Thus, if 14-bit buses will be used, a 7x6 PCB layout will be required. Note also that if the buses will be multi-tapped, the number of layers required will go down, and some vacant layers can be used as ground planes to shield sensitive components from EMI.

5. Conclusions

(a) The bus population and bus width affect the FPGA package size which will be used
(b) More buses will mean more freedom in the addressing sequence.
(c) More buses will mean less DAC's are affected if a bus line fails.
(d) More buses will not require much more routing time.
(e) More buses will not increase the firmware complexity, because the firmware is already required to function with an interleaved bus pattern.
(f) More buses will mean more noise, but measures can be taken to control this
(g) A wider bus will mean less flexibility in PCB routing. However, a 7x6 configuration offers enough space to route full 14-bit buses.
(h) Although 8 bit-wide buses are sufficient for accuracy, there is no harm and little work required to make them wider. This will result in a more flexible design.
(i) If the LSBs of a 14-bit bus will not be used, they will not inject more noise into the AC because they can be directly terminated to ground through the FPGA. In fact, by doing this, one would reduce the noise in adjacent bus lines, and reduce bounce and sag.

In consideration of the points above, **it is proposed that 11 14-bit-wide buses be used**. This is the most intensive 14-bit bus scheme that can be managed by all FPGAs in the 780-pin family. This scheme will use 165 of 292 I/O pins available on the EP1S10 for addressing. Each bus will have 4 DACs multi-tapped from it except the dark-row-DAC bus. An EP1S10 will have enough I/O to segregate bus lines and reduce bounce and sag. This scheme also reduces to 4 the number of DACs affected by the failure of a bus. It will allow the AC to select any one of 37 other DACs while deselecting one.

The best physical layout for DACs is in a 7x6 configuration. This configuration will not encroach on the digital portion of the AC, and it will provide enough spacing between DAC columns to comfortably route a full 14-bit bus on a single layer.