Extender Card Description

Introduction

1.1 Purpose

This document is an analysis of the extender card (EC) requirements. It is to be used as a guideline for the design and as an agent for communication.

1.2 Scope

This document will be a record of what was discussed and agreed upon in regards to the interfaces and functionality of the EC by the warm electronics group at UBC. This document will be adhered to during hardware design.

1.3 Overview

The EC is to be used exclusively for testing purposes. When inserted, the board it is attached to it is extended outside of the sub rack which allows for testing of the card of interest.

2. General description

The EC is used to extend one of 10 cards in each subrack of SCUBA-2 warm electronics. Each subrack will be responsible for the control and data acquisition of one quadrant of a detector array in the cryostat.

2.1 Product Functions

The EC will physically extend the card of interest (one of CC, AC, RC) from being level with the backplane, to being above the plane of the subrack, thus allowing for testing of the card. This must be accomplished without compromising the operation of any of the cards within the subrack.

2.2 User Problem Statement

The essential problem that the EC will solve is that of testing and debugging of individual cards once they are in the subracks.

3. Functional Requirements

In the following section, the functional requirements of the EC are listed. Functional requirements describe what the EC will accomplish. Other kinds of requirements (such as interface requirements, performance requirements, or reliability requirements) describe *how* the EC accomplishes its functional requirements, and will be discussed later.

3.1 Physical Clearance of Card and SubRack

- Description: The EC will move the card completely clear of the subrack.
- Criticality: High
- Technical issues: The current subrack has locking pins, which clip on the inside of the subrack and therefore block any extender type card. The extender card will have to be designed with these clips outside of the subrack to allow for the extender card to raise the card being tested above the subrack.
- Risks: As the connectors have 100 pins, the physical force required to attach and separate them could be quite excessive.

3.2 Proper Transmission of signals

- Description: The EC should correctly transmit the signals from the backplane to the card being tested.
- Criticality: High
  Technical issues: The extender card must transmit the signals from the backplane to the card without allowing any of the signals to be compromised. The most volatile of these transmissions are the LVDS lines and so they must be run close together in order to pick up similar amounts of noise.
- Risks: Running 192 lines across the extender card could lead to interference.

4. Design constraints

4.1 Standards Compliance

- **IEEE**
  1076 VHDL Language Reference Manual
- **LVDS**
  National Semiconductor Owners Manual

4.2 Hardware Limitations

- Digital circuitry should be physically and electrically separated from analog circuitry. In general, because the noisy digital circuitry could have unexpected effects on the low-noise analog circuitry, the two will be physically separate from each other on the
- Ground planes will be extensive. Ground connections between different planes will be jumped, so that they can be separated if necessary.
- Board size limitations will be: 6U high; 4-6HP wide; 250 mm deep
- LVDS signals should run as striplined pairs. This will reduce EMR from the traces. At NIST, the ground/return stripline is wider than the signal stripline.

4.3 Testing & Diagnostic Hardware

The following hardware will be used for testing and debugging the EC. Note that this is not an exhaustive list.

- Windows 2000 Development and Configuration Computer
- Labview
- Workbench
- Storage Space
- Oscilloscope
- Function Generator
- Subrack populated with working PC and CC

5. ENGINEERING DECISIONS

5.1. GENERAL

Several meetings between MCE engineers were held at UBC in order to determine the functionality of the extender card and to specify the best design approach.

5.2. PASSIVE CARD

The best design option is to build a passive extender card. An active card was considered which would drive the LVDS lines, but was discarded because of the difficulty of designing an extender card which would be universal to each individual card if they were driven. The main problem came from the fact that the clock card is primarily sending signals and all the other cards primarily receive signals. This would mean that the signals would need to be driven in different directions depending upon which card the extender was attached to. Thus, the extender would have to be "intelligent" – able to detect which card it is plugged into – or we would have to design different extender cards for each different card. This could lead to problems during testing if the cards get mixed up. The desire is to keep the project as simple as possible.

5.3. POWER CARD CONCERNS

Extending the power card presented some problems. Most of the other cards have similar backplane pin configurations (relatively) but the power card is considerably different. This makes designing one extender card much more difficult and risky. Also, there are some lines on the power card that do not match up well with mapping them to the matching lines on other cards.

The power card is on the far right side of the subrack, which led the project engineers to realize that the power card could be tested and accessed without the need of an extender. For this reason and the reasons listed above the, the extender card will not be compatible with the power card. Leaving the power card to be tested on its own while in the subrack.

5.4. LVDS CONCERNS

The LVDS lines are the signals with which the most care must be taken. The lines run in pairs and work by identifying the differences between the two lines. It is therefore important that the lines run very close together on the circuit board so that they pick up similar amounts of noise as they cross the circuit board. Another design recommendation is to run the LVDS lines between two ground planes on the circuit board. The LVDS signals have a characteristic impedance of 50 ohms and a differential impedance of 100 ohms. This is determined by the width of the traces and the spacing of the traces to the ground plane, so the ground plane layers help to provide the controlled impedance. The LVDS lines will be run on mid layer 2 and mid layer 4 between ground planes to protect them.