Physics and Astronomy Dept.
UBC
SCUBA-2 Project

Tom Felton
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Bus Backplane Description.

The Bus Backplane (BB) is the circuit board that distributes power and digital signals in the subrack. It is designed to fit in a IEEE-1101 standard Eurocard chassis. The circuit board contains ten 192 pin 2mm Future Bus connectors. The circuit board should be at least 0.100" thick with sufficient mounting screws to reduce circuit board flex when inserting and extracting cards.

Power supply pins and common signal connections are bussed to all cards. Power connections use multiple pins on each card due to the 1 Amp current limitation per pin. Enough pins have been used such that no pin will carry more than half it's rated current and in most cases much less. For this reason the Power Card connector pinouts deviate from the rest of the subrack connectors although the basic signal order is maintained.

The analog power connections are placed near the top of the connector. The digital power and digital signals are placed near the bottom of the connector. This allows a basic separation of digital and analog commons. Digital signals on the backplane are of 3 types. LVDS signals, TTL signals and JTAG signals.

LVDS signals are either bussed to all cards or are a direct connection between the Clock Card and one of the other cards. The LVDS signals are routed as impedance matched differential pairs with appropriate terminations.

The TTL signals are bussed to all cards and have pull-up resistors on the backplane. There are some additional TTL signals between the Clock Card and the Power Supply card to allow them to communicate.

JTAG signals are daisy chained through all plugged in cards. Active circuitry on the backplane determines if a card has been removed and will bypass the JTAG data signal to the next card maintaining JTAG continuity.

Slot identification is provided by hardwire jumpering of slot ID pins on the backplane. These signals may be read by the card plugged into that slot. The bus circuit board itself contains a silicon serial number that is readable by the Clock Card.

The subarray that a particular subrack is connected to is also sensed by the Bus Backplane. A set of optical interrupters are used to read keying information off of the 8 cryostat mounting templates. The keying information is forwarded to the clock card. This allows a subrack to identify which subarray it is connected to and report this information as part of the house keeping data.

Completed schematics, board layout and board layer structure are available for this circuit.