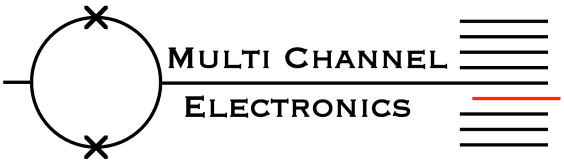

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MCE Bias Card Technical Description

Rev.	Date	Author	Description of change
14.	9 July 2007	William Hue	Add detailed comments on Schematic
15	20 July 2007	MH	Add general terms, remove parts common to all cards and convert to .tex
15.1	3 Aug 2007	MH	Incorporates comments. Still missing Figures.

Abstract: The Bias Card (BC) of the the Multi-Channel Electronics (MCE) developed at the University of British Columbia provides 32 commandable, single ended low noise, low bandwidth voltages to control a three stage squid-based preamplifier. In SCUBA2 electronics, the 32 voltages generated by one bias card provide either the second stage squid bias current, the second stage squid feedback flux or the squid series array feedback flux, depending on which of the three dedicated bias card slots the card has been plugged into. The voltages pass through load resistors located on the instrument bus backplane which define the effective current range. This arrangement allows one design of bias card to perform these three different functions within the electronics, reducing the need for spare cards.

The bias cards also provide a very low noise, double-ended detector bias current or a pixel heater current, again, depending upon slot location.

The low bandwidth requirements of the bias signals permit an extremely low-noise design, which is required for detector operation at very low light levels. The Bias Card receives power and commands and sends replies via the Bus Backplane (BB). Analogue signals are sent from the Bias Card to the cryostat via the Instrument Bus (IB).

Contents

1 Introduction

1.1 Background In a SCUBA2-like array of detectors, the signals detected by the superconducting Transition Edge Sensor (TES) bolometers are amplified by a three-stage SQUID preamplifier and multiplexor.[1] There is one first stage squid per pixel and all the pixels in a given row are turned on at one time by a current from the Address Card.[2] This is time-domain multiplexing. There is one second stage SQUID and one SQUID series array module (SSAM) per column. The TES pixels need to be voltage biased to keep them at the transition temperature and optionally need to be warmed up with the use of an auxiliary pixel heater to compensate different thermal inputs. Each stage of the SQUID amplifier is biased at a current chosen to provide large magnetic flux amplification. Also, each stage of the amplifier has two inputs. One is a signal input and the other is called a feedback input. A bias current provides a flux to this feedback input in order to set the working point of the response at a value corresponding to high slope. In nominal operation the levels of these biases are only varied on very long time scales compared to multiplexing rates and audio frequencies of the radiometric signals.

A Bias Card can provide the bias or feedback signals for the second stage squid or the feedback signals for the squid series array modules.[3] Which of these functions it does perform depends on the cards location within the electronics chassis. Any one bias card provides 32 commandable values, one for each column. Additionally, the bias cards provide a very low noise commandable signal to bias the TES array or to provide current to the pixel heaters.

The BC inserted into the BC1 slot is responsible for:

- SQUID Series Array (SSAM) Feedback (SSA_FB): A DC voltage generates a flux applied to the input of the squid series array module. This value is chosen to hold the SSAM in a region of high slope after the bias in the second stage squid has been set.
- The double ended bias is not used in slot 3.

The BC inserted into the BC2 slot is responsible for:

- 2nd Stage SQUID Feedback (S2_FB): A DC current is applied to generate a flux offset to each of 32 second stage SQUID feedback inputs, to bias them to the linear part of their voltage-flux response curve. Typically, this value is chosen after the first stage squid bias current has been determined.
- Detector Bias (DET_BIAS): A commandable DC voltage brings the detector elements to the midpoint of the superconducting transition. The detector bias is set

at a fixed level during observation or swept through a range of values to collect a detector bias curve. For SCUBA2, the single Detector Bias voltage is applied to the whole sub-array.

The BC inserted into the BC3 slot is responsible for:

- Second Stage SQUID Bias (S2_BIAS): Provides the current-bias for the 2nd stage SQUIDs. This bias is chosen to maximize the slope in the second stage squid V-Phi curve.
- Heater Bias (PXL_HTR): Provides up to 300pW of peak auxiliary heating power per TES pixel. There is one Heater value per sub-array and it is rarely altered much in operation. .

2 Functional Description

Every bias card in the MCE can provide 32 single ended voltages and a small number of other bias voltages. What these voltages are used for is determined by which slot the Bias Card has been inserted into. The signal routing and load resistors which determine the function and current are located on the Instrument Bus (IB) backplane. In SCUBA2, three BCs are required per 32x41 pixel sub-array, which is a quadrant of the full single passband array. The main part of the digital control logic is encapsulated in a 780-pin Altera Stratix FPGA, which allows vertical migration between EP1S10-EP1S40 devices. In SCUBA2 we use EPS10 devices on the Bias Cards.

Each BC receives its commands from the CC through the BB LVDS communications channels and returns data to the CC upon command.

2.1 32 Single-Ended Bias Outputs

The BC provides 32 single-ended analogue outputs. In SCUBA-2, these will be used for providing the 2nd-stage feedback, 2nd-stage SQUID bias and series array feedback currents. Each output is generated by a serial-input, voltage-output, 16-bit DAC (Max5443) with a high-stability (1 ppm/C), low-noise, +2.5 V voltage reference (U18, U19). Upon reset or power up, all the DACs are set to 0. The output of the DAC is buffered by a low-noise operational amplifier (U25 for DAC1), which then drives a bias resistor to generate a bias current. Each channels total bias resistance is the sum of the a load resistor on the BC, an additional load resistor on the IB, and the resistance of the cryogenic cable and other connections and loads in the subarray. See Table 1.

2.2 Ultra Low-Noise, Differential, Pseudo-Isolated Bias Output

The BC provides two pairs of differential outputs generated from **one** active circuit. One output pair is configured as a detector bias, while the other is configured as a pixel heater.[4] Each output pair has its own current-setting load resistors. Due to the common active circuit, only one output pair can be used on any one card; in any given BC Slot only one output pair or the other, or neither, is connected to the backplane.

The differential output circuitry uses a single serial-input, voltage-output, 16-bit DAC (U36) with its own voltage reference and regulators. The digital interface to the DAC is semi-isolated via an LVDS transmitter and receiver pair. The DACs output is converted to differential voltages by two high-precision, very low-noise operational amplifiers (U16A, U17A). The differential output pairs are lowpass-filtered to 10 kHz and fed to high-impedance, low-noise, high-stability (10 ppm) bias resistors. The current ranges are described in Table 2

2.3 Flux-Purge Outputs The BC also provides two current-limited outputs (SSA_HTR) switched 0 to 5V to power heater resistors optionally mounted near the series arrays for the purpose of purging trapped flux. The output current is not adjustable, but is under the control of the FPGA upon command from the CC.[5] This operation has **never been tested** cryogenically and the necessary heater circuit is not implemented within the SCUBA2 cryostat.

2.4 Power Requirements The BC regulates its own power rails from the subracks +Vah, +Va, -Va, +Vlvd and +Vcore busses. The +Vlvd and +Vcore supplies are not monitored directly by the FPGA, as faults on either of these two supplies would already cause reset and/or shutdown of the FPGA through the hardware reset/watchdog circuit. The maximum rated power consumption is 6.24W. In normal use the BC is measured to consume 2.58W.

2.5 Synchronisation with Addressing and Readout In all supported operating conditions to date, the BC provides static or very slowly varying outputs to the

Table 1: Bias Card Current Limits

Slot: Function	R_L on BC (Ω)	R_L on IBB (Ω)	Cryo Load (Ω)	Current Max. (μA)	Resolution (nA)
1: SSA_FB	200 Ω	4.99 kΩ	265 Ω	458 μA	7
2: S2_FB	200 Ω	10 kΩ	265 Ω	239 μA	3.6
3: S2_BIAS	200 Ω	2 kΩ	265 Ω	1014 μA	15.5

detector and SQUID arrays. Changes in bias values usually take place while the MCE is not actively reporting data from the arrays. However, the BC has provision for accepting and using the BB Syncp/Syncn signal pair[6] , should it be necessary to synchronise with addressing and readout activities. Additional firmware would be required.

2.6 Features in common with other cards

The features listed below are common to all cards in the MCE with little variation. These features are documented in more detail elsewhere[7] . Where small distinctions exist between the BC and other cards we have commented.

2.6.1 Bus Backplane Communications

The BB communications is based on a Command-Reply model with the Clock Card acting as the master. Communication from the Clock Card to all the slave cards is via a single set of LVDS line pairs which go to all cards in series. All cards return data to the Clock Card via 16 LVDS lines which are wired point to point. The commands identify the target card, and may include data. The responses may be simple acknowledgments, or may include other information. The BC assumes a unique address based on its slot-identifier code, and uses this code to recognize commands on the input LVDS lines. More information on BB Communications is found in documents the references.[10]

2.6.2 Slot Identification, Silicon ID and Firmware Version

The BC reads a slot-identity from a pattern of short circuits on the Bus Backplane (BB). The slot-identifier code is used by the FPGA firmware to form the BCs BB communications protocol address (see section 2.6.1, allowing the CC to manage multiple BCs, and to associate particular BCs with particular functions.

An on-board silicon identifier device (a Maxim DS18S20) provides a unique serial number, and the FPGA firmware itself will contain a firmware version identifier. These three items can be reported to the CC upon command.

Table 2: Detector Bias and Heater Currents

Slot: Function	R_{Load} on BC (Ω)	R_{Load} on IBB (Ω)	Cryo Load (Ω)	Max. Current (μA)	Resolution (nA)
1: Detector Bias	14 k	0	265	351	5.3
2: Pixel Heater	250 k	0	265	20	0.30

2.6.3 Sense Temperatures The silicon identifier on each BC has an on-board temperature sensor. Additionally, the die temperature of the BCs FPGA is monitored using the FPGAs on-chip, diode-connected transistor and a helper chip. These temperatures are reported upon command.

2.6.4 FPGA Configuration and JTAG Interface An enhanced flash-based configuration device (EPC16) is used to configure the Stratix FPGA device upon power-up or reset. The JTAG interface is used to program both the configuration device and the FPGA. The BCs FPGA and configuration device are included in the subracks internal JTAG chain; the BB contains logic to bypass these devices if a card is not present The JTAG interface can be controlled from either the CCs Front-Panel JTAG Connector or the PC which controls the mCE. It takes less than 2 seconds for the FPGA to load the configuration after the BB BRst signal is released.

3 Hardware

This section describes, in detail, the BC circuit implementation. This section is organized to match the pagination of the schematic diagram.[9] Some BB signals have slightly different names than on the Bias Card schematic, and will be referred to by their BB names with their Bias Card names in parentheses.

3.1 Bias Card Sheet 1: Interfaces

3.1.1 Instrumentation Bus Connector (J1) All analogue outputs from the BC are brought to the IB through J1. Each single-ended signal has a separate return line, routed on the circuit board so that it forms a 50-ohm transmission line with its corresponding signal line, back to AGND at the DAC and buffer the signal comes from. Differential outputs have return lines that come from an amplifier output, rather than AGND.

3.1.2 Power Supply Voltages on Bus_Backplane connector J2 The BC uses several supply voltages from the BB for its digital and analogue circuitry. The Bias Card drops the BB supply voltages through linear regulators to ensure correct voltage and noise requirements are met. The +Vlvd (+Vlvd) and +Vcore (+Vcore) supplies are used to power the digital I/O circuits and FPGA core, respectively. They feed on-board regulators on Sheet 6. The +Vah, +Va and -Va supplies are used for the analogue circuits on Sheets 3, 6 and 8.

U1A and associated components form a voltage comparator with a threshold of approximately 11.34 V and a small amount of hysteresis. This circuit is intended to pull n15VOK low when the +Vah supply is deemed sufficient. However, the new PSUs +Vah output is only about +10 V, so this circuit requires component-value changes to work properly.

U1B and associated components form a voltage comparator with a threshold of approximately -6.46 V and a small amount of hysteresis. This circuit is intended to set MINUS7VOK high when the -Va supply is deemed sufficient. However, the new PSUs -Va output is only about -6.2 to -6.5 V, so this circuit requires component-value changes to work properly.

U2B and associated components form a voltage comparator with a threshold of approximately 5.88 V and a small amount of hysteresis. This circuit is intended to pull n7VOK low when the +Va supply is deemed sufficient.

3.1.3 LVDS Receivers and Transmitters U3 and U5 are the LVDS receivers for the bussed BB signals from the CC. These devices are located very close to J2 on the BC circuit board in order to minimise stub length on the LVDS busses. U4 is the LVDS transmitter for the two dedicated communication channels back to the CC.

3.1.4 Other BB Interfaces U8 buffers the SIDx (nSIDx) and nExtnd (nEXTEND) signals, with ESD protection from R99 and R101-R104; these resistors are large, 1206, packages to discourage arc-over of the ESD charge. U9 and U7 create the interface to the bi-directional SpTTLx and BClr (BCLR) BB signals. Note that BClr (BCLR) was originally a bi-directional SpTTLx signal, and was reassigned to be an output from the CC and an input on all the other cards (except for the PSU) in the subrack.

The BRst (BRST) and JTAG (TCK, TDI, TDO, TMS) signals go to Sheet 2. The note about a narrow ground bridge between DGND and AGND is outdated. The revised MCE grounding scheme [9] has a single ground.

3.2 Bias Card Sheet 2: Reset and Configuration

U27 and associated components are the configuration memory circuit for the FPGA, connected in the standard Altera Fast Passive Parallel mode [8]. Under certain circumstances, U27 will hold its nINIT_CONF signal low; D11A prevents this condition from affecting the rest of the BCs circuitry (e.g. holding the DACs in reset via nDAC_CLR). U11 and RN12 provide a fault- and ESD-protected interface to the BB JTAG chain. U28, U29 and associated components form a voltage-detecting reset circuit to reset/reconfigure the FPGA once both I/O and core voltages are stable. R19 directly connects the +1.5VD rail to U28s RST IN pin to determine the reset threshold at 1.22 V. C58 programs U28 to release its /RST

output approximately 30 ms after the +1.5VD rail has stabilised above 1.22 V. U28s /RST output is cascaded to U29, which is programmed by R20, R23 and C61 to release the BCs nRESET signal approximately 3 seconds after the +3.3VD rail has stabilised above 2.96 V. (Note: The RT and WT times shown on the schematic are outdated.)

U28 and U29 also provide a watchdog function for the FPGA. While U28s watchdog is disabled by grounding the SWT pin, U29s watchdog timeout is programmed to 1 second by C5. U28 and U29s reset timeout (SRT) capacitors were chosen to satisfy the FPGAs requirements to ensure reconfiguration regardless of I/O and core voltage sequencing; the timeout values were obtained after a large amount of research, as the FPGAs do not behave exactly as Altera claims. JP1 is normally set to allow CONF_DONE to disable the watchdog, by allowing U29s WDI input to float and self-reset, when the FPGA has not been configured. Once the FPGA has been configured, CONF_DONE goes high and the FPGA must toggle the wdog signal to avoid being reset by the watchdog. JP1 in the grounded position forces the watchdog off during debugging, while R24 ensures the watchdog is enabled if JP1 is not installed.

Push-button SW1 (not accessible from front panel) shunts the voltage from R19 to ground, providing a manual, de-bounced, reset trigger. R22, D6A and D6B provide protection against ESD from the operators finger. Note that R22 is a large, 1206, package to discourage arc-over of the ESD charge.

U2A and associated components form a threshold detector for the BB BRst signal. R15, R17 and C57 create a filtered reference of approximately 1.03 V. This reference, together with R31 and R16 cause U2As output to pull low when BRst (BRST) is above approximately 2.58 V. The damping provided by C56 and the small amount of hysteresis provided by R18 prevent oscillations due to noise. D9A prevents the reference voltage created by R15 and R17 from affecting the divider formed by R20 and R23. Q2B and Q2A generate an open-drain signal on the BB SpTTL4 (ConfRdy) line; the CC uses this signal to tell if any card in the subrack has an unconfigured FPGA. Q1A illuminates D2 only if the BCs FPGA is unconfigured.

3.3 Bias Card Sheet 3: Ultra low nooise differential bias outputs

This is the differential detector bias or heater drive circuit. It can provide either detector bias or pixel heater drive; it cannot provide both outputs independently at once. The differential bias output is required to be very low noise [7]. Thus, it is necessary for the differential drive circuit to have its own power supplies rather than sharing power with the circuitry for the single-ended bias outputs. U34, U35 and associated components create the 5 V supplies dedicated to the differential output buffers. D13 and D14 ensure that the regulator outputs do not get reverse-biased by more than one Schottky diode-drop. U35, in particular, will latch in a fault mode if its output pin is lifted positive due to return current from the powered circuitry; this condition can present itself if U34s output comes up faster than U35s output. U36 is a serial-input, voltage-output, 16-bit DAC with its own voltage reference U32 and regulator U33. Control signals come

from the FPGA via low-noise LVDS signals and LVDS receivers U14 and U15. U36s 6.2 kilohm output impedance, R57 and C154 band-limit the DAC output signal to 11.5 kHz (10 kHz nominal) before being buffered by U16. U17 generates the complement of the buffered DAC output; gain-setting resistors R59 and R60 are high-precision, high-stability, low-noise types. The 2.5 V DAC reference voltage yields a full-scale differential voltage swing of 5 V. U16 and U17 were chosen from the ultra-low noise LT1028/LT1128 family; the LT1128 was used as it was unity-gain stable. The two operational amplifier outputs then drive ultra low noise, metal-foil type bias resistors; the capacitors provide more shaping of the noise spectrum. The components shown as DNP provide for additional bias resistors and capacitors, depending on the application and availability of resistor values.

3.4 Bias Card Sheet 4

The serial interface signals to the BCs DACs originate from U6B, U6C and U6D. U6F provides the control signals for the flux-purge heater outputs and the LVDS control signals (using the FPGAs built-in LVDS transmitters) for the differential bias outputs.

U6A provides connections to the BB interfaces, and the front-panel LEDs (D3-D5). Note that D3 is wired so that it is illuminated (albeit at a lower intensity) if the FPGA is not driving the red_led signal; an illuminated red LED indicates that a card is powered, but has a fault. U30 is the on-board combined temperature-sensor/silicon-identifier chip.

P1 is a general-purpose debugging header. P2 is an impedance-controlled, Mictor type header which can be used for high-speed logic analysis. P3 is a dedicated interface for an external RS-232 serial line interface for card-debugging purposes. Push-button SW2 and associated circuitry provide an ESD-protected manual register-reset input for the BCs FPGA. Note that the FPGA firmware must be programmed to use the FPGAs DEV_CLRn input as a register-reset input in order for SW2 to have any effect.

3.5 Bias Card Sheet 5: FPGA Clock distribution, Configuration and Power

3.5.1 Clock Distribution

U37 is a special low-skew clock driver device used to fan-out the BB LVDS clock source to all the FPGA clock inputs. The FPGAs internal PLLs and clock domains have certain restrictions on which clock-input pins may be used to drive certain internal resources; 2 clock-input pins are required to implement the BCs required functionality.

3.5.2 FPGA I/O Power, PLL Outputs, Configuration Signals, Die Temperature Sensor

An elaborate power-decoupling scheme is shown on U6I. The capacitors

are distributed in a carefully-planned pattern on the circuit board to reduce power-rail bounce and I/O ringing. While the scheme shown does not completely eliminate simultaneous-switching noise (SSN) when a large number of FPGA I/O pins are switching at the same time, it is sufficient for the firmware the BC runs in the MCE.

Also on U6I is the FPGAs dedicated pins for selecting the configuration mode, and the FPGAs hardware JTAG signals. SW3 controls the FPGAs configuration mode selection signals, and also provides two general-purpose input switches (signals dip_sw3 and dip_sw4).

The FPGA contains an on-die, diode-connected, transistor for use as a temperature sensor. U31 is a helper chip specifically designed to convert the silicon-junction forward-bias voltage to an SMBus data stream. The FPGA firmware reads the die temperature to ensure overheating damage does not occur in case of subrack ventilation failure.

3.5.3 FPGA Core and PLL Power U6Js VCCINT pins are connected to an elaborate power-distribution mesh similar to the FPGAs VCCIOx pins; similar care was taken in the circuit board layout to ensure proper FPGA core operation. Note the additional inductive filtering for the FPGA PLL +1.5 V power pins. This technique is recommended by Altera to provide additional isolation between the PLLs, and between the PLLs and the FPGA core. Although no PLL outputs are used in the BC, the PLL output power pins must still be connected to +3.3 V; the filters formed by L502, L503 and associated capacitors are overkill, and sharing the VCCIOx distribution network would likely have been sufficient.

3.6 Bias Card Sheet 6

3.6.1 Analogue References and Voltage Regulators U18 and U19 are the precision, high-stability voltage references for the 32 single-ended bias output DACs. Two references due to the limited output-current capability of the MAX6325 reference chip. U20 provides the +3.3 V supply to all 32 single-ended bias output DACs. U20 is fed from the same power rail (+Vah) as the references, to comply with the DACs requirement that their +3.3 V supply and reference voltage are available at the same time.

U21 and U23 provide the 5 V power rails for the single-ended bias outputs buffer amplifiers. These two regulators also power the flux-purge heater outputs. D7 and D8 ensure that the regulator outputs do not get reverse-biased by more than one Schottky diode-drop. U23, in particular, will latch in a fault mode if its output pin is lifted positive due to return current from the powered circuitry; this condition can present itself if U21s output comes up faster than U23s output.

3.6.2 Single-Ended Bias Output Sub-Circuits The 16 blocks labelled BC_Channel.SCHDOC each represent one instance of the circuitry on Sheet 7. A bug in the schematic CAD software causes the CH designators to have no numeric suffix, but the channel numbers can be determined by the numbered input (control) signals to each block.

3.6.3 FPGA I/O and Core Voltage Regulators, Chassis Grounding U22 and U24 are low-dropout, high-current, regulators providing the +3.3 V and +1.5 V power rails, respectively. They are protected against input transients and noise by TS2, L6, TS4, L7, and have multiple input and output capacitors to ensure stability. Aluminium-organic and/or tantalum-organic capacitors are used for low-ESR without the short-circuit failure mechanism of regular tantalum capacitors. Additionally, the +3.3 V rail is prevented from being lifted above approximately 3.6 V by D1, as could happen if any of the BB SpTTLx (and other BB) signals are driven by 5-volt logic.

R1-R3, distributed around the BCs card-edge contact rails, permit controlled ESD charge equalisation between the subrack chassis and the BC circuitry during card insertion and removal. TS5 and TS6 limit the chassis-to-circuit voltage differential to a safe level; for low voltage differentials, the resistors provide a soft equalisation while the transient suppressor diodes ensure a fast discharge of larger voltages.

3.7 Bias Card Sheet 7: Single-Ended Bias Outputs

This schematic sheet is the implementation of two single-ended bias output circuits, which is replicated 16 times by the blocks on Sheet 6. Two serial-input, 16-bit, MAX5443 DACs each share one amplifier in a dual OPA2227 device. Each DACs 6.2 kilohm output impedance combined with R7/R12 and C42/C46 form a 2.5 kHz lowpass filter. R5/R10 and C47/C48 provide further roll-off at 8 kHz.

3.8 Bias Card Sheet 8

U38 and U41 are high-current, rail-to-rail operational amplifiers with internal current-limiting and indefinite short-circuit capability; they are used solely to provide current-limiting of the 5 V sources for the flux-purge heater outputs. (Excessive current will damage the ADG619 switches, and/or parts of the array.) Two pairs of SPDT analogue switches (U39/U40, U42/U43) allow the FPGA to control the application of 5 V to a pair of outputs to the IB connector (J1). A total of 10 V gives enough current through any length of cryogenic cable to bring SQuIDs out of superconductivity to clear trapped flux. Termination resistors R125, R128, R130 and R132 control noise when the heaters are not active.

3.9 Bias Card Sheet 9

This schematic sheet shows the output utilisation of three BCs and an IB as used in SCUBA2.

4 Firmware:

The firmware on the FPGA controls the following external devices: 32 + 1 serial DACs (MAX5443) to set bias values, the id/thermo chip(DS1820) to read the silicon ID and temperature, 3 front-panel LEDs to report the card status.

A 25MHz clock coming across the backplane is used as the input to the FPGA PLL to generate the internal FPGA 50MHz clock along with the 100MHz clock used for over-sampling required for backplane communication.

The backplane communication is also handled by the firmware where incoming commands (over the multi-drop LVDS pair) are received by lvds_rx block and processed by dispatch block; subsequently a reply in accordance with SC2_ELE_58x_xxx[10] is generated and sent by the lvds_tx block (down one of the 2 dedicated point-to-point LVDS pairs on the backplane) to CC.

The backplane communication link is a 50MHz serial asynchronous link. The receiving block, lvds_rx, samples data at 100MHz (2x of the transmission rate) to recover the data. For details, see lvds_rx doc and lvds_tx doc.

The dispatch block identifies the card (its host) through the slot_id pins and when processing a command only decodes the commands for the identified card. For list of commands supported by each card, see[11] MCE Command Description, SC2_ELE_S580_515. Then the command is passed to the appropriate firmware block and a reply is generated.

The Wishbone bus protocol (refer to Wishbone SpecificationXX) is adopted as inter-block communication standard between the different blocks in bias_card. One block, in this case dispatch, acts as Wishbone Master and the other blocks are Wishbone slaves. The slave blocks are:

- `bc_dac_ctrl` to handle **flux_fb** and **bias** commands to set biases by loading all serial 16b DACs with values specified in the command. Refer to [bc_dac_ctrl.doc]. Upon receiving the command all values are registered and then loaded into the DACs one after next upon start of a data frame.

  The internal 50MHz clock is divided down by 4 to load the serial DACs at 12.5MHz. It takes 16×80ns = 1280ns to load each DAC and since they are loaded one after next, it takes 32×1280ns + 32×80ns (overhead) = 43.5μs to load all the DACs. See Figure x for timing information.

- `frame_timing` to handle all commands related to the frame structure, so it can generate an `update_bias_o` signal that indicates the beginning of a data frame.

- `id_thermo` to handle **card_id** and **card_temp** commands and to retrieve the silicon and the temperature from DS1820 chip. Refer to [thermo_id.doc]

- `fw_rev` to return the firmware revision.
- `leds` to to handle the **led** command and to load the LEDs with the values specified in the command.
- `fpga_thermo` to handle fpga_temp command and to retrieve the temperature readings of the FPGA on-chip temperature sensor accessory.
- slot_id to handle the **slot_id** command and return the backplane identification number.

Table 3: Bias Card Commands

Parameter	**Description**
flux_fb	Takes 32 unsigned values between 0 to (216-1) to load the 32 16b serial DACs. When out of range values are specified, the 16 lower bits are in effect.
bias	Takes an unsigned value between 0 and $(2^{16} - 1)$ to program the on-board LVDS DAC. When out-of-range values are specified, the 16 lower bits are in effect.
fpga_temp	Retrieve the FPGA silicon temperature through the on-board helper chip.
card_temp	Retrieve the card temperature from on-board DS8020
card_id	Retrieve the silicon ID from on-board DS8020
led	Takes a 3b value to control/toggle the on-board LEDs. The specified value is XORed with current status of LEDs. Therefore, the result of writing 111 to this parameter may vary depending on what the current status of LEDs were at the time.
fw_rev	Returns a firmware revision where the format is `RRrrBBBB` `RR` is the major revision number `rr` is the minor revision number `BBBB` is the build number
slot_id	Returns the 4b ID of the particular slot the card is plugged into.
row_len	Specify number of 50MHz clock cycles per row
num_rows	Specify number of rows per frame
	Together row_len and num_rows allow calculation of the number of 50 MHz clock cycles per frame.

List of Acronyms:

TES	Transition edge superconductor bolometers
SQUID	Super-conducting Quantum Interference Device
MCE	Multi-Channel Electronics
BC	Bias Card
CC	Clock Card
BB	Bus Backplane
IB	Instrumentation Backplane
DAC	Digital to Analogue Converter
FPGA	Field Programmable Gate Array
JTAG	Joint Test Action Group, an industry group who created, and the common name given to, the IEEE 1149.1 standard, Standard Test Access Port and Boundary-Scan Architecture. [Really! When we say JTAG we are not talking about the group!]
PSU	Power Supply Unit
ESD	Electro-Static Discharge
RC	Readout Card
I/O	Input/Output
LVDS	Low-Voltage Differential Signalling
TTL	Transistor-Transistor Logic, and the logical voltage levels used thereby.
CMOS	Complementary Metal-Oxide Semiconductor (logic), and the 5-volt logical voltage levels used thereby.
LVCMOS	Low-Voltage CMOS (logic), and the 2.7- to 3.3-volt logical voltage levels used thereby.
AC	Address Card
SSN	Simultaneous Switching Noise
SPDT	Single-Pole Double-Throw

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