Address Card Technical Description

1. References

[1] 'Using the Jam Language for ISP & ICR via an Embedded Processor' Altera Application Note 088
[2] 'FPGA Configuration Block Diagram' SC2/ELE/S560/003
[3] 'JTAG Bus Switching Circuitry' SC2_ELE_S565_003_007
[4] 'Bus Backplane Connector Pinout' SC2_ELE_S565_001_004
[5] 'SCUBA 2 Protocol – Canada' SC2/SOF/S200/014
[6] 'Multichannel Electronics Requirements and Recommendations' SC2/ELE/S500/011
[7] 'Stratix Device Handbook'
[8] 'Bus Backplane Instruction Set Architecture' SC2_ELE_S565_001_002
[9] 'Bus Backplane ISA Description' SC2_ELE_S565_001_003
[10] 'Address Card DAC Circuitry' SC2_ELE_S565_104_001
[11] 'Multichannel Electronics Block Diagram' SC2/ELE/S560/001
[12] 'Configuring Stratix and Stratix GX Devices' Altera Application Note 208

2. Address Card

2.1 AC Introduction

The AC is the sub-array row-addressing card in each subrack. In SCUBA2's series-address SQUID multiplexer architecture, the AC will produce analog bias currents to turn 'on' one row of 1st stage SQUIDs at a time, using their row-select lines. There are 32 SQUIDs per row, and 41 rows per sub-array. On the AC, the row-select currents are produced by video DACs. The DACs are controlled independently by the AC's FPGA (i.e. 14 data bits + 1 clock signal per DAC).

2.2 AC Engineering Requirements

2.2.1 Prevent Card Insertion in the Wrong Subrack Slot

Refer to CC Engineering Requirements.

2.2.2 Accept Configuration Data from the CC

The Altera devices on the AC will be part of a JTAG chain that meanders through the multi-channel electronics. This will allow users to:

(a) Configure the AC's configuration device (EPC16) while the card is in-circuit,
(b) Extract diagnostic information from the AC's FPGA.

The AC will not provide an on-board JTAG header.

2.2.3 Provide Persistent Storage for FPGA Reconfiguration Data

The AC will store its configuration in an Altera configuration device. The configuration device will be part of the JTAG chain so that it is programmable in-circuit (refer to [2]). During subrack power-up, the AC FPGA will be automatically configured by the configuration device. Reconfiguration may be triggered by JTAG bus commands and/or a 'configuration reset'.

2.2.4 Interface with the BB

The AC's BB connector will be compatible with slot '1' of the BB pinout. The AC pinout is outlined in [4]. A description of the pins is given above in the CC description.

2.2.5 Identify the AC's Own Slot #, Serial # and Firmware Version

Refer to the CC Engineering Requirements.

2.2.6 Receive (Addressing) Commands From the CC

The AC will support a specific command protocol as outlined in [8] and [9].

In particular, the AC will also support a generalized mode of addressing in which it cycles through all or a certain number of rows at a certain rate, until a certain number of frames are complete. In the generalized addressing mode, the actions of the AC will be co-ordinated with those of the RCs and BCs, to ensure that AC and BC lines have settled before SQUID values are read by the RCs. This will be done using a strictly timed internal frame structure that is consistent with the other cards. Then each card would be synchronized externally once every unfiltered/filtered frame or so.

Timing adjustments will be initiated by the CC via the multi-dropped 'Cmd' or 'Sync' line.

The AC may also support addressing commands from the CC that direct it to enable a single row-select for an indefinite period of time.

Synchronization errors will be possible, and may be difficult to diagnose. An intelligent robust testing plan will be necessary.

2.2.7 Reply to All Commands from the CC

The AC will support a specific command protocol as outlined in [8] and [9].

The AC will reply to every command that applies to it, that it receives from the CC. In general, the CC will initiate communication with the AC. This is a simple and robust protocol that fits with the master/slave protocol that was suggested for transmission between the RTL computers and the CC. If, in response to a request from the CC, the AC should return data, then its reply will contain the information requested, otherwise the reply will be a short string. The replies of the AC should be byte-aligned with those of every card.

2.2.8 Detect Transmission Errors from the CC

CC error detection and recovery will be done in the following manner: if the AC receives a garbled request, then its reply will notify the CC that it received an erroneous transmission, and the CC will then re-send the request (to all cards) if necessary.

2.2.9 Select a Row: Simultaneously Maintain Analog Biases to 41 Rows

To select a row, the AC must do the following:

(a) Apply 'off' currents to all rows that will be de-selected (row-to-row nulling currents may differ).
(b) Apply an appropriate biasing current to the row that is to be selected (row-to-row selection currents may differ).

Row-select currents will be generated by 41 14-bit video DACs on the AC. Each DAC will have its own clock-latch input. There will be four DACs sharing each 14-bit data bus. This will make it possible to simultaneously select/deselect certain rows. NIST has said that simultaneous selection/deselection of two rows does not have a dominant effect on the system settling time.

Analog Device AD9744 DACs will be used for row selection. They will be configured as a straight binary, with noise isolating resistors on its inputs.

2.2.10 Provide Diagnostic Information

Refer to the CC Engineering Requirements.

2.2.11 Tap into the JTAG Chain

The JTAG chain has a point-to-point topology. The AC will be a removable link in the JTAG chain. The AC will provide a control signal to divert signals from the chain when it is inserted, and maintain the continuity of the chain when it is not (refer to S565_104_001.schdoc for details). To maintain correct JTAG topology of the chain, the BB 'TCK' and 'TMS' signals will be multi-tapped, and the BB 'TDI' and 'TDO' signals will be diverted.

2.2.12 Sense AC Temperature

The on-board temperature will be sensed with a Maxim temperature-sensor (DS18S20 – this IC will be used simultaneously as a silicon ID). The CC will prompt the AC for its thermal information.

Additionally, the package temperature of the CC FPGA will be monitored using the FPGA's on-board diode-connected transistor and a helper chip.

2.2.13 Interface with the IB/Cryostat

The AC's DACs are specified to supply 0-20 mA with compliance of 1.2V. This requires a total DAC load of 50Ω. Each row-select line contains a bias resister (~5KΩ) to provide 'on'/'off'bias currents for each address line (refer to S565_104_001.schdoc for details). The AC will have 41 row-select channels.

2.2.14 Support Board-Level Resets

For development and debugging purposes, it would be desirable to include on-board reset buttons for to trigger a local (AC only) configuration reset.