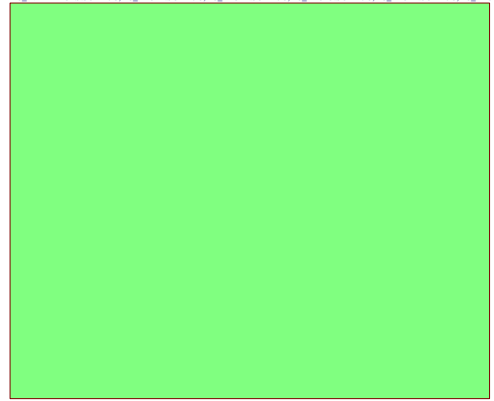


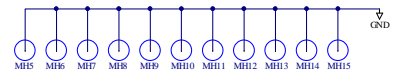
Readout Card - All Sheets
 RC_INTERFACES.SCHDOC;RC_FPGA1.SCHDOC;RC_FPGA2.SCHDOC;RC_FPGA3.SCHDOC;RC_FPGA4.SCHDOC;RC_FPGA5.SCHDOC;RC_FPGA6.SCHDOC;RC_MEMORY.SCHDOC;RC_ANALOGUE.SCHDOC;RC_POWER_SUPPLIES1.SCHDOC;RC_POWER_SUPPLIES2.SCHDOC;RC_Mechanical.SCHDOC



Use UBC Logo
 Use UBC Logo

Add Fiducial Point
 FP1
 Add Fiducial Point
 FP2
 Add Fiducial Point
 FP3
 Add Fiducial Point
 FP4

Etchral fiducials should be located in the four corners of the PCB board.
 Fiducials should be at least 5mm from the edge of the board.

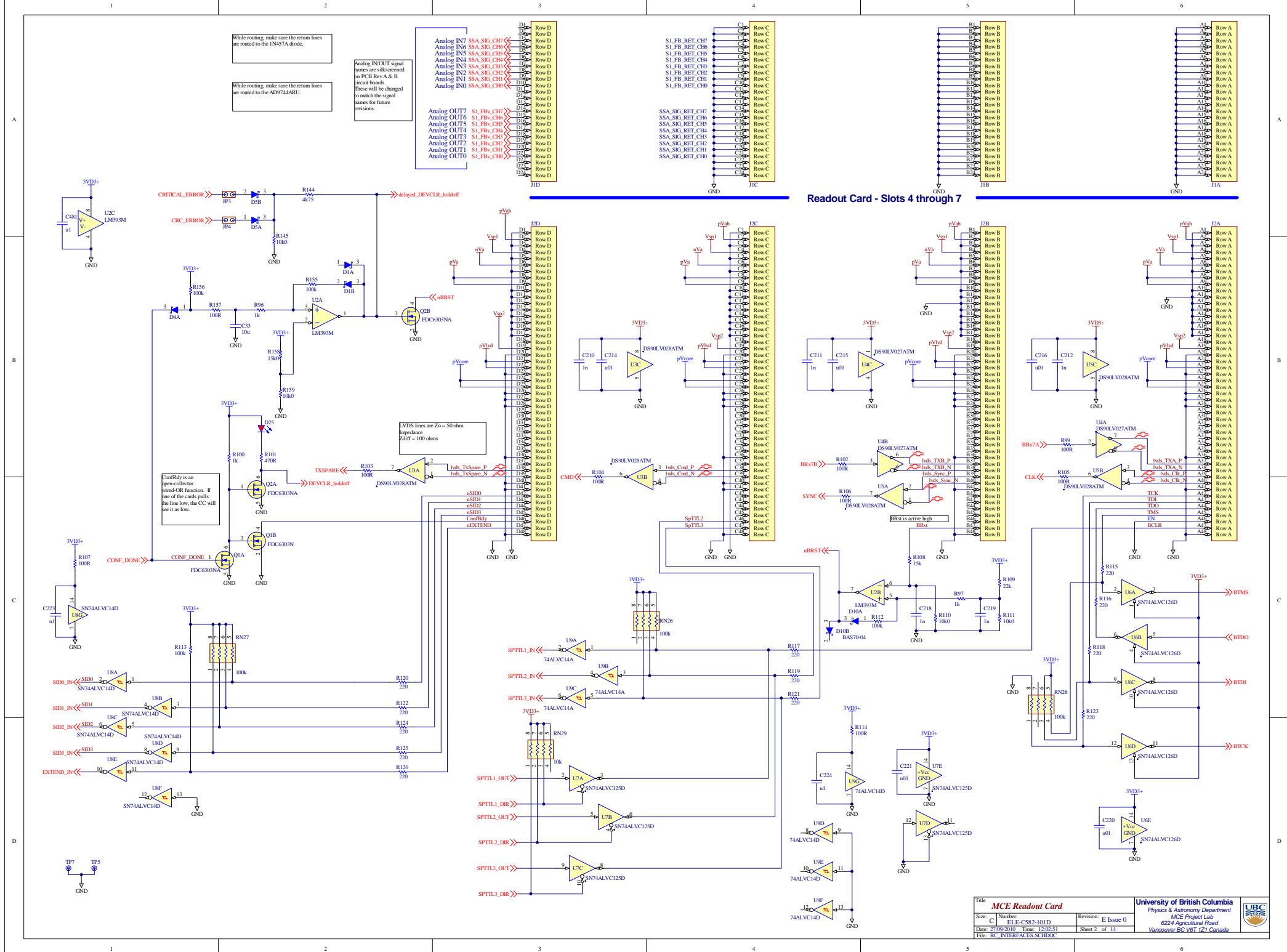


There is a problem with manually placing Mounting Holes. Created Part to fix problem

Front Panel Mounting Assembly

<p style="text-align: center;">Bottom Extraction Handle Manufacturer: Ritral Part Number: 3686-902 Mech3</p>	<p style="text-align: center;">Top Extraction Handle Manufacturer: Ritral Part Number: 3686-903 Mech4</p>
<p style="text-align: center;">SCIBAD Readout Card Front Panel Manufacturer: PHAS-MS Part Number: SC2-ELE-SS81-110 Mech8</p>	<p style="text-align: center;">Mounting Bracket for PCB Manufacturer: Ritral Part Number: 3685-198 (10pack) Mech11</p>
<p style="text-align: center;">Mounting Bracket for PCB Manufacturer: Ritral Part Number: 3685-198 (10pack) Mech12</p>	<p style="text-align: center;">M2.5 x 8mm Machine Screw Cone Head Type: Hardware Mech15</p>
<p style="text-align: center;">M2.5 x 8mm Machine Screw Cone Head Type: Hardware Mech16</p>	<p style="text-align: center;">M2.5 x 8mm Machine Screw Type: Hardware Mech19</p>
<p style="text-align: center;">M2.5 x 8mm Machine Screw Type: Hardware Mech21</p>	<p style="text-align: center;">M2.5 x 8mm Machine Screw Type: Hardware Mech20</p>
<p style="text-align: center;">M2.5 x 8mm Machine Screw Type: Hardware Mech22</p>	<p style="text-align: center;">M2.5 x 8mm Machine Screw Type: Hardware Mech22</p>

PCB Part Number for BOM: ELE-SS84-101E



U10K
BANK 6A

IO, DIFF0_TX_R28a, DIFFOUT_R56a
IO, DIFF0_TX_R28b, DIFFOUT_R56b
IO, RDNSA, DIFF0_RX_R28a, DIFFOUT_R55a
IO, RUP5A, DIFF0_RX_R28a, DIFFOUT_R55a
IO, DIFF0_TX_R27a, DIFFOUT_R54a (DQ14R)(DQ14R)
IO, DIFF0_TX_R27b, DIFFOUT_R54b (DQ14R)(DQ14R)
IO, DIFF0_RX_R27a, DIFFOUT_R53a (DQ8a4R)(DQ14R)(DQ14R)
IO, DIFF0_RX_R27b, DIFFOUT_R53b (DQ8a4R)(DQ14R)(DQ14R)
IO, DIFF0_TX_R26a, DIFFOUT_R52a (DQ14R)(DQ14R)(DQ14R)
IO, DIFF0_TX_R26b, DIFFOUT_R52b (DQ14R)(DQ14R)(DQ14R)
IO, DIFF0_RX_R26a, DIFFOUT_R51a (DQ8a13R)(DQ8a13R)(DQ14R)(DQ14R)
IO, DIFF0_RX_R26b, DIFFOUT_R51b (DQ8a13R)(DQ8a13R)(DQ14R)(DQ14R)
IO, DIFF0_TX_R25a, DIFFOUT_R50a (DQ8a13R)(DQ14R)(DQ14R)
IO, DIFF0_TX_R25b, DIFFOUT_R50b (DQ8a13R)(DQ14R)(DQ14R)
IO, DIFF0_RX_R25a, DIFFOUT_R49a (DQ13R)(DQ14R)(DQ14R)
IO, DIFF0_RX_R25b, DIFFOUT_R49b (DQ13R)(DQ14R)(DQ14R)
IO, DIFF0_TX_R24a, DIFFOUT_R48a (DQ13R)(DQ14R)(DQ14R)
IO, DIFF0_TX_R24b, DIFFOUT_R48b (DQ13R)(DQ14R)(DQ14R)
IO, DIFF0_RX_R24a, DIFFOUT_R47a (DQ8a12R)(DQ13R)(DQ8a12R)(DQ14R)(DQ14R)
IO, DIFF0_RX_R24b, DIFFOUT_R47b (DQ8a12R)(DQ13R)(DQ8a12R)(DQ14R)(DQ14R)
IO, DIFF0_TX_R23a, DIFFOUT_R46a (DQ12R)(DQ13R)(DQ14R)
IO, DIFF0_TX_R23b, DIFFOUT_R46b (DQ12R)(DQ13R)(DQ14R)
IO, DIFF0_RX_R23a, DIFFOUT_R45a (DQ8a11R)(DQ8a11R)(DQ13R)(DQ14R)
IO, DIFF0_RX_R23b, DIFFOUT_R45b (DQ8a11R)(DQ8a11R)(DQ13R)(DQ14R)
IO, DIFF0_TX_R22a, DIFFOUT_R44a (DQ11R)(DQ13R)(DQ14R)
IO, DIFF0_TX_R22b, DIFFOUT_R44b (DQ11R)(DQ13R)(DQ14R)
IO, DIFF0_RX_R22a, DIFFOUT_R43a (DQ11R)(DQ13R)(DQ14R)
IO, DIFF0_RX_R22b, DIFFOUT_R43b (DQ11R)(DQ13R)(DQ14R)
IO, DIFF0_TX_R21a, DIFFOUT_R42a
IO, DIFF0_TX_R21b, DIFFOUT_R42b
IO, DIFF0_RX_R21a, DIFFOUT_R41a
IO, DIFF0_RX_R21b, DIFFOUT_R41b
IO, DIFF0_TX_R20a, DIFFOUT_R40a
IO, DIFF0_TX_R20b, DIFFOUT_R40b

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U100
BANK 8A

IO, DIFF0_TX_T64a (DQ17T)(DQ17T)(DQ17T)
IO, DIFF0_TX_T64b (DQ17T)(DQ17T)(DQ17T)
IO, RDNSA, DIFF0_RX_T32a, DIFFOUT_T63a (DQ8a17T)(DQ17T)(DQ17T)
IO, RUP5A, DIFF0_RX_T32a, DIFFOUT_T63a (DQ8a17T)(DQ17T)(DQ17T)
IO, DIFF0_TX_T62a (DQ17T)(DQ17T)(DQ17T)
IO, DIFF0_TX_T62b (DQ17T)(DQ17T)(DQ17T)
IO, DIFF0_TX_T61a (DQ8a16T)(DQ8a16T)(DQ17T)(DQ17T)
IO, DIFF0_TX_T61b (DQ8a16T)(DQ8a16T)(DQ17T)(DQ17T)
IO, DIFF0_RX_T61a, DIFFOUT_T60a (DQ16T)(DQ17T)(DQ17T)
IO, DIFF0_RX_T61b, DIFFOUT_T60b (DQ16T)(DQ17T)(DQ17T)
IO, DIFF0_TX_T59a, DIFFOUT_T59a (DQ16T)(DQ17T)(DQ17T)
IO, DIFF0_TX_T59b, DIFFOUT_T59b (DQ16T)(DQ17T)(DQ17T)
IO, DIFF0_RX_T59a, DIFFOUT_T58a (DQ16T)(DQ17T)(DQ17T)
IO, DIFF0_RX_T59b, DIFFOUT_T58b (DQ16T)(DQ17T)(DQ17T)
IO, DIFF0_TX_T57a (DQ8a15T)(DQ8a15T)(DQ8a15T)(DQ17T)(DQ17T)
IO, DIFF0_TX_T57b (DQ8a15T)(DQ8a15T)(DQ8a15T)(DQ17T)(DQ17T)
IO, DIFF0_RX_T57a, DIFFOUT_T56a (DQ15T)(DQ16T)(DQ17T)
IO, DIFF0_RX_T57b, DIFFOUT_T56b (DQ15T)(DQ16T)(DQ17T)
IO, DIFF0_TX_T55a, DIFFOUT_T55a (DQ15T)(DQ16T)(DQ17T)
IO, DIFF0_TX_T55b, DIFFOUT_T55b (DQ15T)(DQ16T)(DQ17T)
IO, DIFF0_RX_T55a, DIFFOUT_T54a (DQ14T)(DQ16T)(DQ17T)
IO, DIFF0_RX_T55b, DIFFOUT_T54b (DQ14T)(DQ16T)(DQ17T)
IO, DIFF0_TX_T53a, DIFFOUT_T53a (DQ14T)(DQ16T)(DQ17T)
IO, DIFF0_TX_T53b, DIFFOUT_T53b (DQ14T)(DQ16T)(DQ17T)
IO, DIFF0_RX_T53a, DIFFOUT_T52a (DQ8a14T)(DQ8a14T)(DQ16T)(DQ17T)
IO, DIFF0_RX_T53b, DIFFOUT_T52b (DQ8a14T)(DQ8a14T)(DQ16T)(DQ17T)
IO, DIFF0_TX_T51a (DQ8a13T)(DQ8a13T)(DQ15T)(DQ17T)
IO, DIFF0_TX_T51b (DQ8a13T)(DQ8a13T)(DQ15T)(DQ17T)
IO, DIFF0_RX_T51a, DIFFOUT_T50a (DQ15T)(DQ16T)(DQ17T)
IO, DIFF0_RX_T51b, DIFFOUT_T50b (DQ15T)(DQ16T)(DQ17T)
IO, DIFF0_TX_T49a, DIFFOUT_T49a (DQ15T)(DQ16T)(DQ17T)
IO, DIFF0_TX_T49b, DIFFOUT_T49b (DQ15T)(DQ16T)(DQ17T)
IO, DIFF0_RX_T49a, DIFFOUT_T48a (DQ14T)(DQ16T)(DQ17T)
IO, DIFF0_RX_T49b, DIFFOUT_T48b (DQ14T)(DQ16T)(DQ17T)
IO, DIFF0_TX_T47a, DIFFOUT_T47a (DQ14T)(DQ16T)(DQ17T)
IO, DIFF0_TX_T47b, DIFFOUT_T47b (DQ14T)(DQ16T)(DQ17T)
IO, DIFF0_RX_T47a, DIFFOUT_T46a (DQ8a12T)(DQ8a12T)(DQ16T)(DQ17T)
IO, DIFF0_RX_T47b, DIFFOUT_T46b (DQ8a12T)(DQ8a12T)(DQ16T)(DQ17T)
IO, DIFF0_TX_T45a, DIFFOUT_T45a (DQ13T)(DQ15T)(DQ17T)
IO, DIFF0_TX_T45b, DIFFOUT_T45b (DQ13T)(DQ15T)(DQ17T)
IO, DIFF0_RX_T45a, DIFFOUT_T44a (DQ13T)(DQ15T)(DQ17T)
IO, DIFF0_RX_T45b, DIFFOUT_T44b (DQ13T)(DQ15T)(DQ17T)
IO, DIFF0_TX_T43a, DIFFOUT_T43a (DQ13T)(DQ15T)(DQ17T)
IO, DIFF0_TX_T43b, DIFFOUT_T43b (DQ13T)(DQ15T)(DQ17T)
IO, DIFF0_RX_T43a, DIFFOUT_T42a (DQ8a11T)(DQ8a11T)(DQ15T)(DQ17T)
IO, DIFF0_RX_T43b, DIFFOUT_T42b (DQ8a11T)(DQ8a11T)(DQ15T)(DQ17T)
IO, DIFF0_TX_T41a, DIFFOUT_T41a (DQ12T)(DQ15T)(DQ17T)
IO, DIFF0_TX_T41b, DIFFOUT_T41b (DQ12T)(DQ15T)(DQ17T)
IO, DIFF0_RX_T41a, DIFFOUT_T40a (DQ12T)(DQ15T)(DQ17T)
IO, DIFF0_RX_T41b, DIFFOUT_T40b (DQ12T)(DQ15T)(DQ17T)

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Add Fiducial Point
FP5
Add Fiducial Point
FP6

Please locate fiducials
near the BGA footprint.

U10M
BANK 7A

IO, DIFF0_TX_T1a (DQ1T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T1b (DQ1T)(DQ1T)(DQ1T)
IO, RDNSA, DIFF0_RX_T1a, DIFFOUT_T2a (DQ8a1T)(DQ1T)(DQ1T)
IO, RUP5A, DIFF0_RX_T1a, DIFFOUT_T2a (DQ8a1T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T1a, DIFFOUT_T2a (DQ8a1T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T1b, DIFFOUT_T2b (DQ8a1T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T1a, DIFFOUT_T1a (DQ8a1T)(DQ8a1T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T1b, DIFFOUT_T1b (DQ8a1T)(DQ8a1T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T2a, DIFFOUT_T3a (DQ8a2T)(DQ8a2T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T2b, DIFFOUT_T3b (DQ8a2T)(DQ8a2T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T2a, DIFFOUT_T2a (DQ8a2T)(DQ8a2T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T2b, DIFFOUT_T2b (DQ8a2T)(DQ8a2T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T3a, DIFFOUT_T4a (DQ8a3T)(DQ8a3T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T3b, DIFFOUT_T4b (DQ8a3T)(DQ8a3T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T3a, DIFFOUT_T3a (DQ8a3T)(DQ8a3T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T3b, DIFFOUT_T3b (DQ8a3T)(DQ8a3T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T4a, DIFFOUT_T5a (DQ8a4T)(DQ8a4T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T4b, DIFFOUT_T5b (DQ8a4T)(DQ8a4T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T4a, DIFFOUT_T4a (DQ8a4T)(DQ8a4T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T4b, DIFFOUT_T4b (DQ8a4T)(DQ8a4T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T5a, DIFFOUT_T6a (DQ8a5T)(DQ8a5T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T5b, DIFFOUT_T6b (DQ8a5T)(DQ8a5T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T5a, DIFFOUT_T5a (DQ8a5T)(DQ8a5T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T5b, DIFFOUT_T5b (DQ8a5T)(DQ8a5T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T6a, DIFFOUT_T7a (DQ8a6T)(DQ8a6T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T6b, DIFFOUT_T7b (DQ8a6T)(DQ8a6T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T6a, DIFFOUT_T6a (DQ8a6T)(DQ8a6T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T6b, DIFFOUT_T6b (DQ8a6T)(DQ8a6T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T7a, DIFFOUT_T8a (DQ8a7T)(DQ8a7T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T7b, DIFFOUT_T8b (DQ8a7T)(DQ8a7T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T7a, DIFFOUT_T7a (DQ8a7T)(DQ8a7T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T7b, DIFFOUT_T7b (DQ8a7T)(DQ8a7T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T8a, DIFFOUT_T9a (DQ8a8T)(DQ8a8T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T8b, DIFFOUT_T9b (DQ8a8T)(DQ8a8T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T8a, DIFFOUT_T8a (DQ8a8T)(DQ8a8T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T8b, DIFFOUT_T8b (DQ8a8T)(DQ8a8T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T9a, DIFFOUT_T10a (DQ8a9T)(DQ8a9T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T9b, DIFFOUT_T10b (DQ8a9T)(DQ8a9T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T9a, DIFFOUT_T9a (DQ8a9T)(DQ8a9T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T9b, DIFFOUT_T9b (DQ8a9T)(DQ8a9T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T10a, DIFFOUT_T11a (DQ8a10T)(DQ8a10T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T10b, DIFFOUT_T11b (DQ8a10T)(DQ8a10T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T10a, DIFFOUT_T10a (DQ8a10T)(DQ8a10T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T10b, DIFFOUT_T10b (DQ8a10T)(DQ8a10T)(DQ1T)(DQ1T)

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U10L
BANK 6C

IO, DIFF0_TX_R25a, DIFFOUT_R40a
IO, DIFF0_TX_R25b, DIFFOUT_R40b
IO, DIFF0_RX_R25a, DIFFOUT_R39a (DQ8a10R)(R) (R)
IO, DIFF0_RX_R25b, DIFFOUT_R39b (DQ8a10R)(R) (R)
IO, DIFF0_TX_R19a, DIFFOUT_R38a (DQ8a9R)(R) (R)
IO, DIFF0_TX_R19b, DIFFOUT_R38b (DQ8a9R)(R) (R)
IO, DIFF0_RX_R19a, DIFFOUT_R37a (DQ8a8R)(R) (R)
IO, DIFF0_RX_R19b, DIFFOUT_R37b (DQ8a8R)(R) (R)
IO, DIFF0_TX_R18a, DIFFOUT_R36a (DQ8a7R)(R) (R)
IO, DIFF0_TX_R18b, DIFFOUT_R36b (DQ8a7R)(R) (R)
IO, DIFF0_RX_R18a, DIFFOUT_R35a (DQ8a6R)(R) (R)
IO, DIFF0_RX_R18b, DIFFOUT_R35b (DQ8a6R)(R) (R)
IO, DIFF0_TX_R17a, DIFFOUT_R34a (DQ8a5R)(R) (R)
IO, DIFF0_TX_R17b, DIFFOUT_R34b (DQ8a5R)(R) (R)
IO, DIFF0_RX_R17a, DIFFOUT_R33a (DQ8a4R)(R) (R)
IO, DIFF0_RX_R17b, DIFFOUT_R33b (DQ8a4R)(R) (R)
IO, DIFF0_TX_R16a, DIFFOUT_R32a (DQ8a3R)(R) (R)
IO, DIFF0_TX_R16b, DIFFOUT_R32b (DQ8a3R)(R) (R)
IO, DIFF0_RX_R16a, DIFFOUT_R31a (DQ8a2R)(R) (R)
IO, DIFF0_RX_R16b, DIFFOUT_R31b (DQ8a2R)(R) (R)
IO, PULL_R2_CLK0T0, DIFF0_TX_R15a, DIFFOUT_R30a
IO, PULL_R2_CLK0T0, DIFF0_TX_R15b, DIFFOUT_R30b
IO, CLK11a, DIFF0_RX_R15a, DIFFOUT_R29a
IO, CLK11a, DIFF0_RX_R15b, DIFFOUT_R29b
IO, DIFF0_TX_R9a, DIFFOUT_R17a
IO, DIFF0_TX_R9b, DIFFOUT_R17b
IO, DIFF0_RX_R9a, DIFFOUT_R16a (DQ8a8R)(R) (R)
IO, DIFF0_RX_R9b, DIFFOUT_R16b (DQ8a8R)(R) (R)
IO, DIFF0_TX_R10a, DIFFOUT_R19a (DQ8a9R)(R) (R)
IO, DIFF0_TX_R10b, DIFFOUT_R19b (DQ8a9R)(R) (R)
IO, DIFF0_RX_R10a, DIFFOUT_R18a (DQ8a8R)(R) (R)
IO, DIFF0_RX_R10b, DIFFOUT_R18b (DQ8a8R)(R) (R)
IO, DIFF0_TX_R11a, DIFFOUT_R21a (DQ8a10R)(R) (R)
IO, DIFF0_TX_R11b, DIFFOUT_R21b (DQ8a10R)(R) (R)
IO, DIFF0_RX_R11a, DIFFOUT_R20a (DQ8a9R)(R) (R)
IO, DIFF0_RX_R11b, DIFFOUT_R20b (DQ8a9R)(R) (R)
IO, DIFF0_TX_R12a, DIFFOUT_R23a (DQ8a11R)(R) (R)
IO, DIFF0_TX_R12b, DIFFOUT_R23b (DQ8a11R)(R) (R)
IO, DIFF0_RX_R12a, DIFFOUT_R22a (DQ8a10R)(R) (R)
IO, DIFF0_RX_R12b, DIFFOUT_R22b (DQ8a10R)(R) (R)
IO, DIFF0_TX_R13a, DIFFOUT_R25a (DQ8a12R)(R) (R)
IO, DIFF0_TX_R13b, DIFFOUT_R25b (DQ8a12R)(R) (R)
IO, DIFF0_RX_R13a, DIFFOUT_R24a (DQ8a11R)(R) (R)
IO, DIFF0_RX_R13b, DIFFOUT_R24b (DQ8a11R)(R) (R)
IO, DIFF0_TX_R14a, DIFFOUT_R27a (DQ8a13R)(R) (R)
IO, DIFF0_TX_R14b, DIFFOUT_R27b (DQ8a13R)(R) (R)
IO, DIFF0_RX_R14a, DIFFOUT_R26a (DQ8a12R)(R) (R)
IO, DIFF0_RX_R14b, DIFFOUT_R26b (DQ8a12R)(R) (R)
IO, CLK0p, DIFF0_RX_R14a, DIFFOUT_R28a
IO, CLK0p, DIFF0_RX_R14b, DIFFOUT_R28b

EP5SE0F780CAN

U10J
BANK 5C

IO, DIFF0_TX_R9a, DIFFOUT_R17a
IO, DIFF0_TX_R9b, DIFFOUT_R17b
IO, DIFF0_RX_R9a, DIFFOUT_R16a (DQ8a8R)(R) (R)
IO, DIFF0_RX_R9b, DIFFOUT_R16b (DQ8a8R)(R) (R)
IO, DIFF0_TX_R10a, DIFFOUT_R19a (DQ8a9R)(R) (R)
IO, DIFF0_TX_R10b, DIFFOUT_R19b (DQ8a9R)(R) (R)
IO, DIFF0_RX_R10a, DIFFOUT_R18a (DQ8a8R)(R) (R)
IO, DIFF0_RX_R10b, DIFFOUT_R18b (DQ8a8R)(R) (R)
IO, DIFF0_TX_R11a, DIFFOUT_R21a (DQ8a10R)(R) (R)
IO, DIFF0_TX_R11b, DIFFOUT_R21b (DQ8a10R)(R) (R)
IO, DIFF0_RX_R11a, DIFFOUT_R20a (DQ8a9R)(R) (R)
IO, DIFF0_RX_R11b, DIFFOUT_R20b (DQ8a9R)(R) (R)
IO, DIFF0_TX_R12a, DIFFOUT_R23a (DQ8a11R)(R) (R)
IO, DIFF0_TX_R12b, DIFFOUT_R23b (DQ8a11R)(R) (R)
IO, DIFF0_RX_R12a, DIFFOUT_R22a (DQ8a10R)(R) (R)
IO, DIFF0_RX_R12b, DIFFOUT_R22b (DQ8a10R)(R) (R)
IO, DIFF0_TX_R13a, DIFFOUT_R25a (DQ8a12R)(R) (R)
IO, DIFF0_TX_R13b, DIFFOUT_R25b (DQ8a12R)(R) (R)
IO, DIFF0_RX_R13a, DIFFOUT_R24a (DQ8a11R)(R) (R)
IO, DIFF0_RX_R13b, DIFFOUT_R24b (DQ8a11R)(R) (R)
IO, DIFF0_TX_R14a, DIFFOUT_R27a (DQ8a13R)(R) (R)
IO, DIFF0_TX_R14b, DIFFOUT_R27b (DQ8a13R)(R) (R)
IO, DIFF0_RX_R14a, DIFFOUT_R26a (DQ8a12R)(R) (R)
IO, DIFF0_RX_R14b, DIFFOUT_R26b (DQ8a12R)(R) (R)
IO, CLK0p, DIFF0_RX_R14a, DIFFOUT_R28a
IO, CLK0p, DIFF0_RX_R14b, DIFFOUT_R28b

EP5SE0F780CAN

U10P
BANK 8C

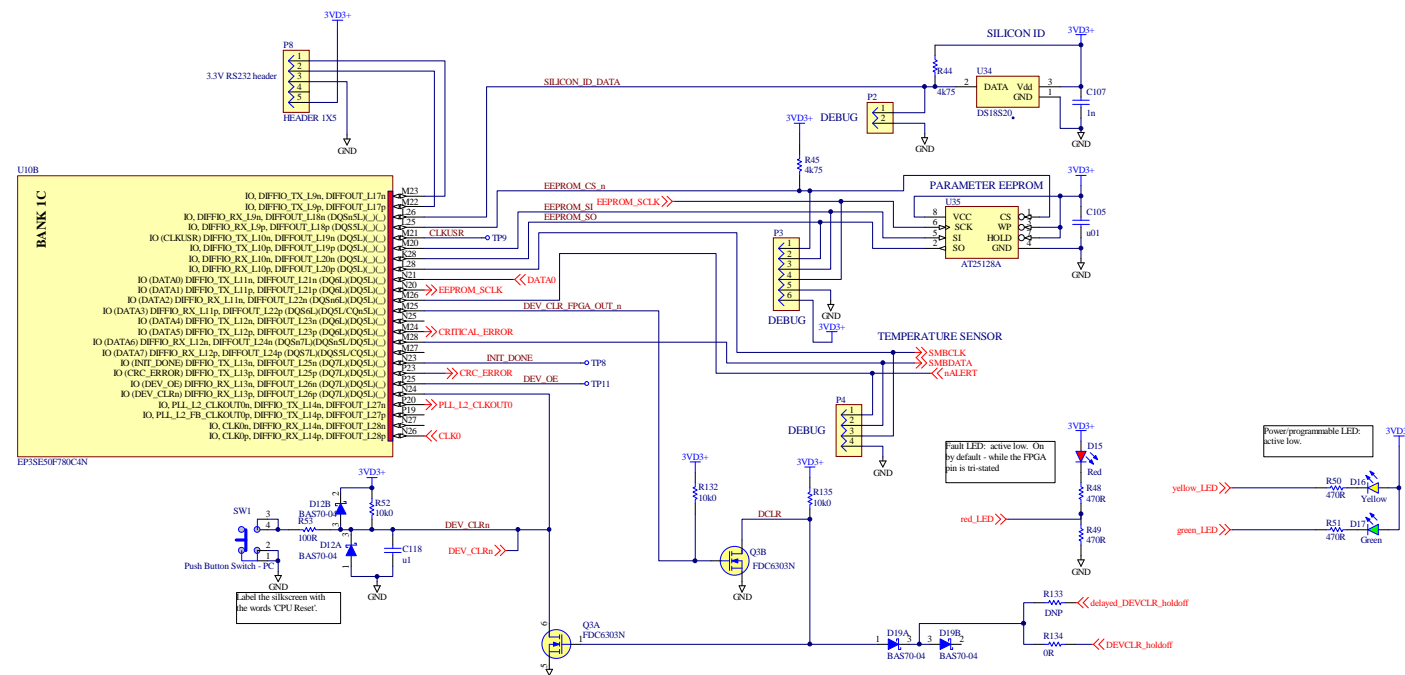
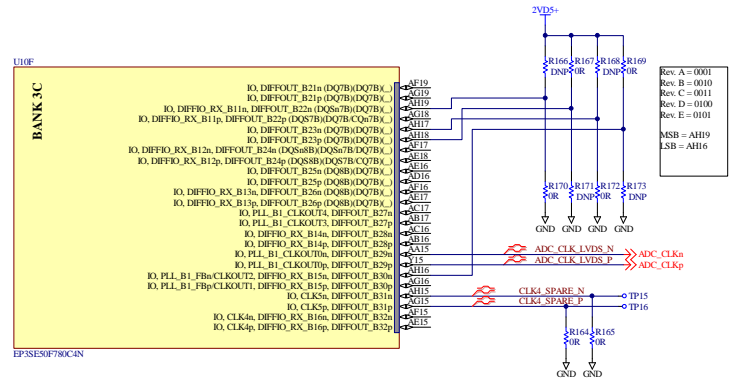
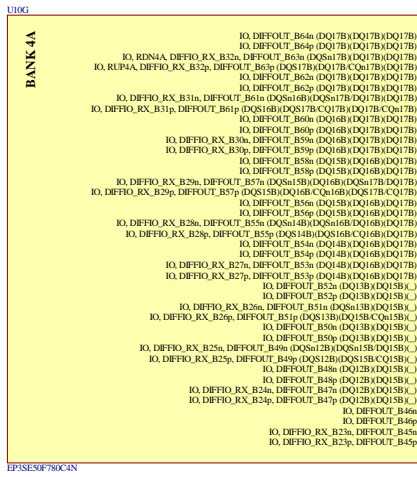
IO, DIFF0_TX_T44a (DQ1T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T44b (DQ1T)(DQ1T)(DQ1T)
IO, RDNSA, DIFF0_RX_T22a, DIFFOUT_T43a (DQ8a11T)(DQ1T)(DQ1T)
IO, RUP5A, DIFF0_RX_T22a, DIFFOUT_T43a (DQ8a11T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T22a, DIFFOUT_T43a (DQ8a11T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T22b, DIFFOUT_T43b (DQ8a11T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T22a, DIFFOUT_T42a (DQ8a10T)(DQ8a10T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T22b, DIFFOUT_T42b (DQ8a10T)(DQ8a10T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T21a, DIFFOUT_T41a (DQ8a9T)(DQ8a9T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T21b, DIFFOUT_T41b (DQ8a9T)(DQ8a9T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T21a, DIFFOUT_T40a (DQ8a8T)(DQ8a8T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T21b, DIFFOUT_T40b (DQ8a8T)(DQ8a8T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T20a, DIFFOUT_T39a (DQ8a7T)(DQ8a7T)(DQ1T)(DQ1T)
IO, DIFF0_TX_T20b, DIFFOUT_T39b (DQ8a7T)(DQ8a7T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T20a, DIFFOUT_T38a (DQ8a6T)(DQ8a6T)(DQ1T)(DQ1T)
IO, DIFF0_RX_T20b, DIFFOUT_T38b (DQ8a6T)(DQ8a6T)(DQ1T)(DQ1T)
IO, PULL_T1_CLK0T0, DIFF0_TX_T19a, DIFFOUT_T37a
IO, PULL_T1_CLK0T0, DIFF0_TX_T19b, DIFFOUT_T37b
IO, PULL_T1_CLK0T0, DIFF0_TX_T18a, DIFFOUT_T35a
IO, PULL_T1_CLK0T0, DIFF0_TX_T18b, DIFFOUT_T35b
IO, CLK15a, DIFFOUT_T34a
IO, CLK15a, DIFFOUT_T34b
IO, CLK14a, DIFF0_RX_T17a, DIFFOUT_T33a
IO, CLK14a, DIFF0_RX_T17b, DIFFOUT_T33b

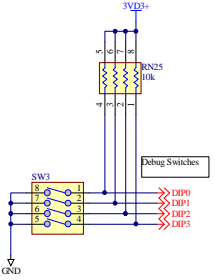
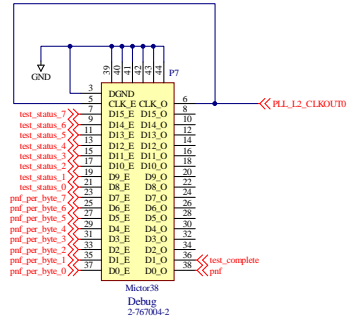
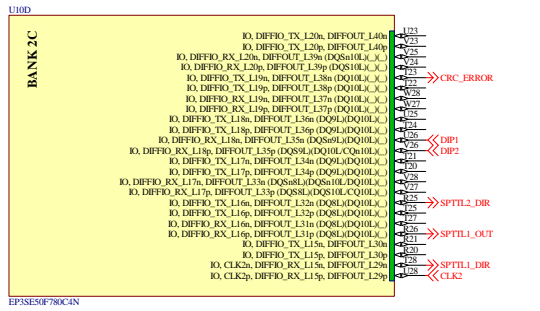
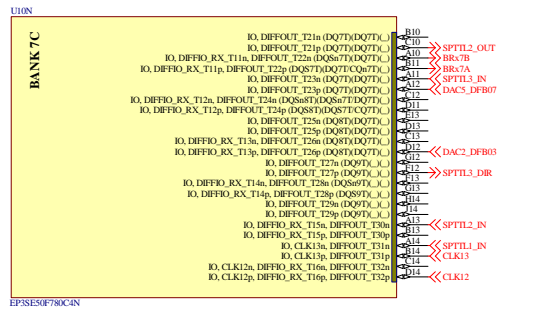
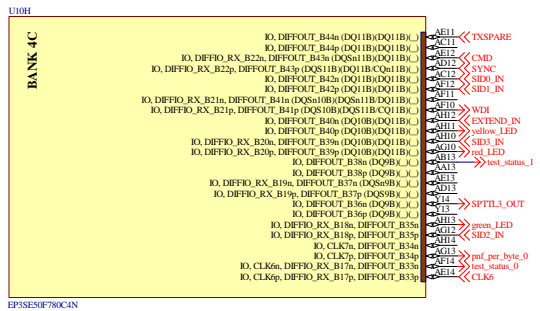
EP5SE0F780CAN

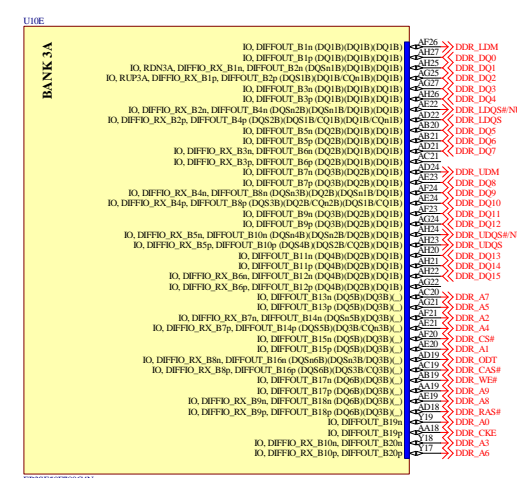
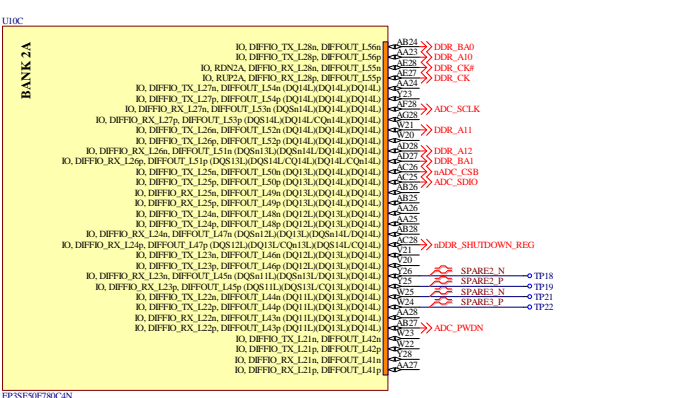
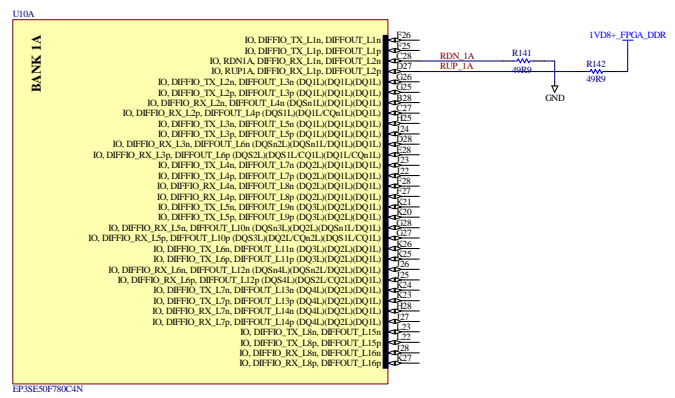
U10H
BANK 5A

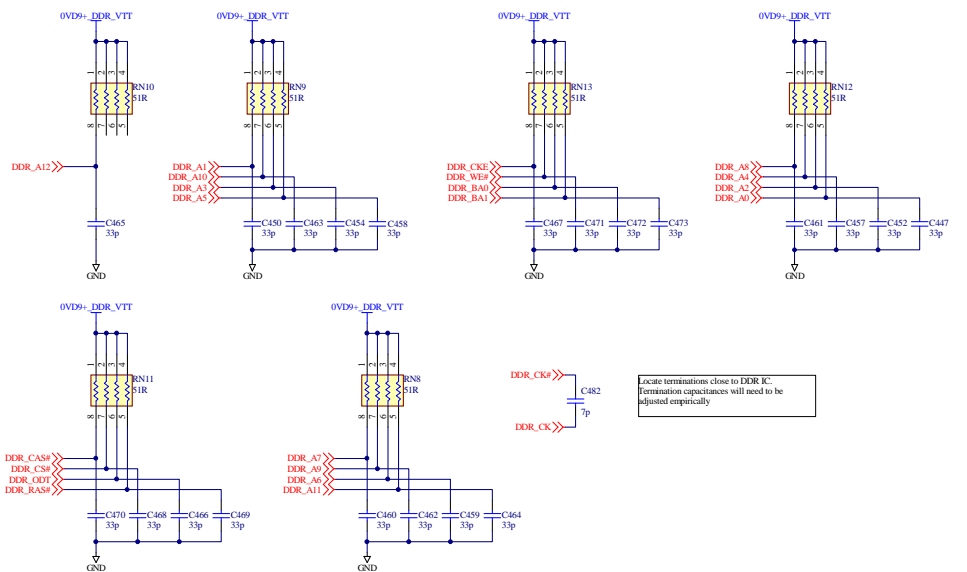
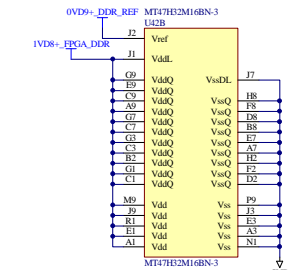
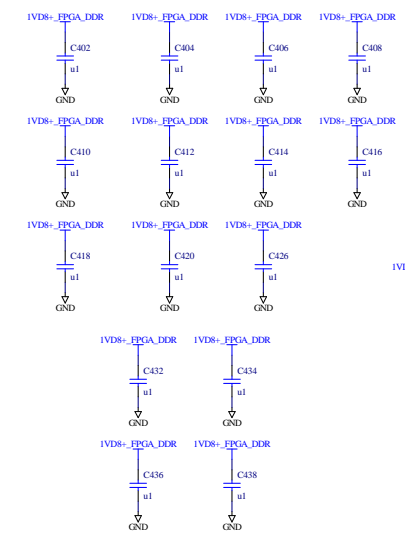
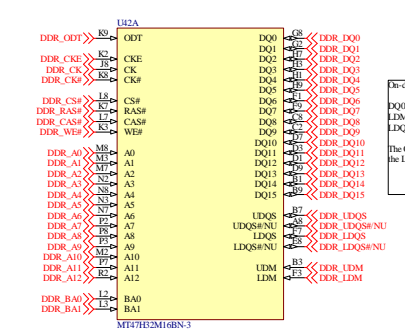
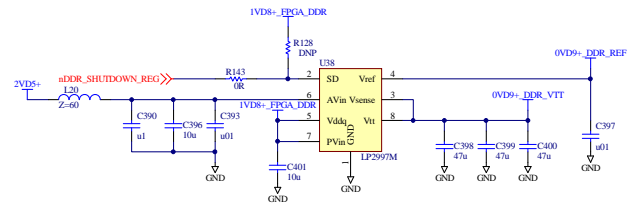
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IO, DIFF0_TX_R1b, DIFFOUT_R1b
IO, RDNSA, DIFF0_RX_R1a, DIFFOUT_R2a
IO, RUP5A, DIFF0_RX_R1a, DIFFOUT_R2a
IO, DIFF0_TX_R2a, DIFFOUT_R3a (DQ1R)(DQ1R)(DQ1R)
IO, DIFF0_TX_R2b, DIFFOUT_R3b (DQ1R)(DQ1R)(DQ1R)
IO, DIFF0_RX_R2a, DIFFOUT_R2a (DQ8a1R)(R) (R)
IO, DIFF0_RX_R2b, DIFFOUT_R2b (DQ8a1R)(R) (R)
IO, DIFF0_TX_R3a, DIFFOUT_R4a (DQ8a2R)(R) (R)
IO, DIFF0_TX_R3b, DIFFOUT_R4b (DQ8a2R)(R) (R)
IO, DIFF0_RX_R3a, DIFFOUT_R3a (DQ8a1R)(R) (R)
IO, DIFF0_RX_R3b, DIFFOUT_R3b (DQ8a1R)(R) (R)
IO, DIFF0_TX_R4a, DIFFOUT_R5a (DQ8a3R)(R) (R)
IO, DIFF0_TX_R4b, DIFFOUT_R5b (DQ8a3R)(R) (R)
IO, DIFF0_RX_R4a, DIFFOUT_R4a (DQ8a2R)(R) (R)
IO, DIFF0_RX_R4b, DIFFOUT_R4b (DQ8a2R)(R) (R)
IO, DIFF0_TX_R5a, DIFFOUT_R6a (DQ8a4R)(R) (R)
IO, DIFF0_TX_R5b, DIFFOUT_R6b (DQ8a4R)(R) (R)
IO, DIFF0_RX_R5a, DIFFOUT_R5a (DQ8a3R)(R) (R)
IO, DIFF0_RX_R5b, DIFFOUT_R5b (DQ8a3R)(R) (R)
IO, DIFF0_TX_R6a, DIFFOUT_R7a (DQ8a5R)(R) (R)
IO, DIFF0_TX_R6b, DIFFOUT_R7b (DQ8a5R)(R) (R)
IO, DIFF0_RX_R6a, DIFFOUT_R6a (DQ8a4R)(R) (R)
IO, DIFF0_RX_R6b, DIFFOUT_R6b (DQ8a4R)(R) (R)
IO, DIFF0_TX_R7a, DIFFOUT_R8a (DQ8a6R)(R) (R)
IO, DIFF0_TX_R7b, DIFFOUT_R8b (DQ8a6R)(R) (R)
IO, DIFF0_RX_R7a, DIFFOUT_R7a (DQ8a5R)(R) (R)
IO, DIFF0_RX_R7b, DIFFOUT_R7b (DQ8a5R)(R) (R)
IO, DIFF0_TX_R8a, DIFFOUT_R9a (DQ8a7R)(R) (R)
IO, DIFF0_TX_R8b, DIFFOUT_R9b (DQ8a7R)(R) (R)
IO, DIFF0_RX_R8a, DIFFOUT_R8a (DQ8a6R)(R) (R)
IO, DIFF0_RX_R8b, DIFFOUT_R8b (DQ8a6R)(R) (R)

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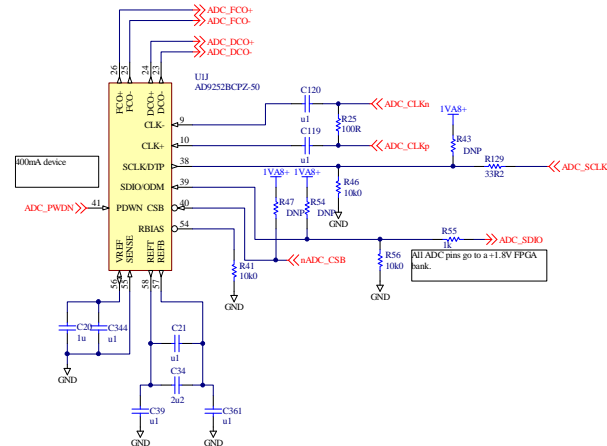
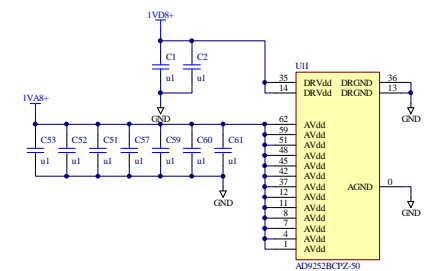
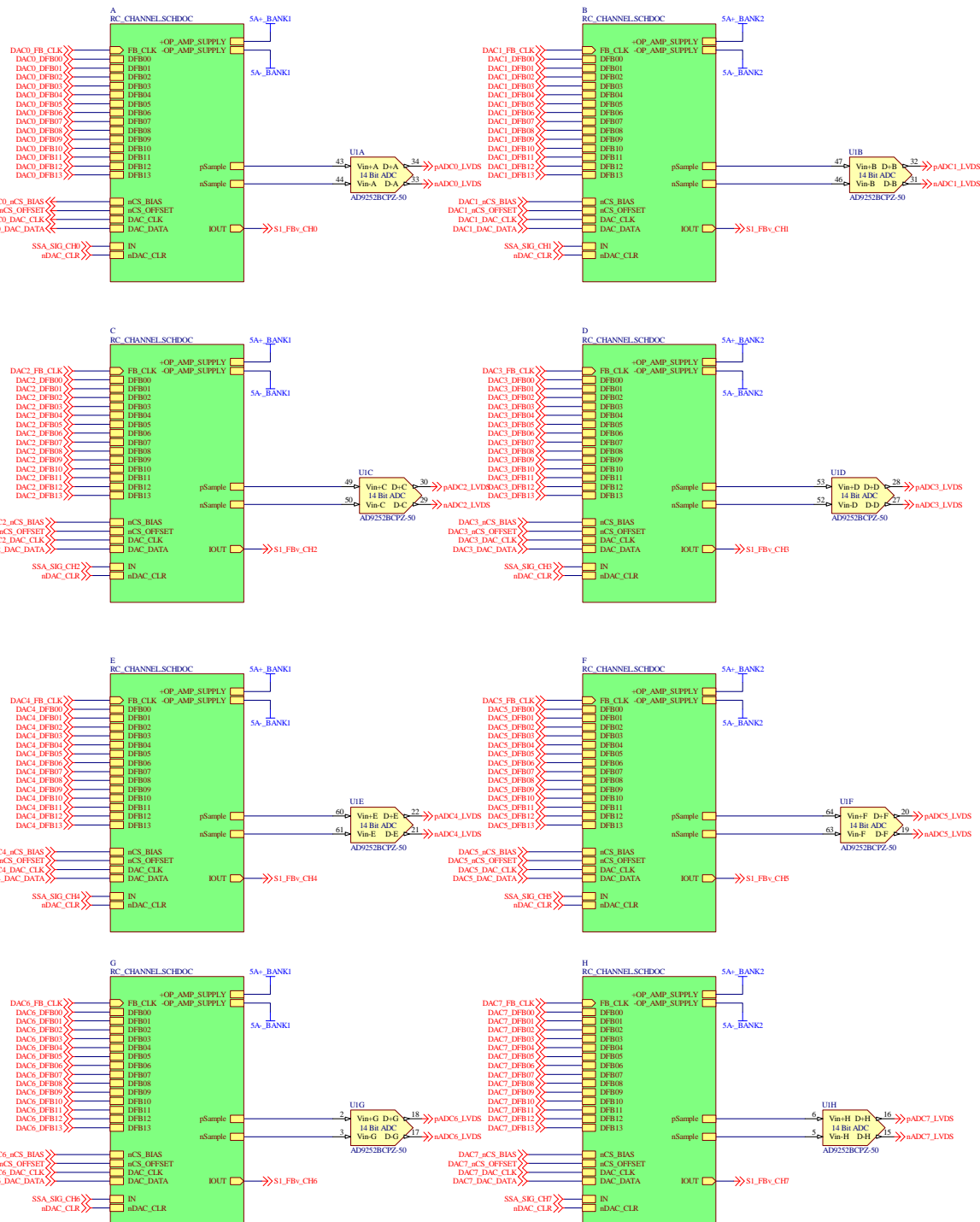


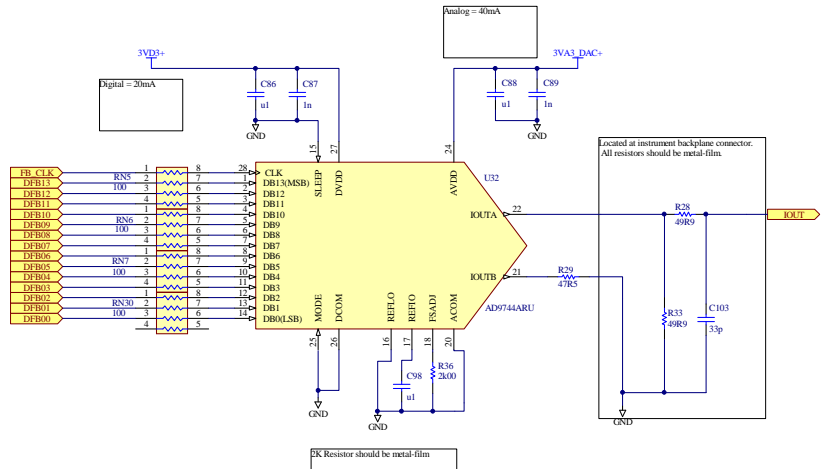
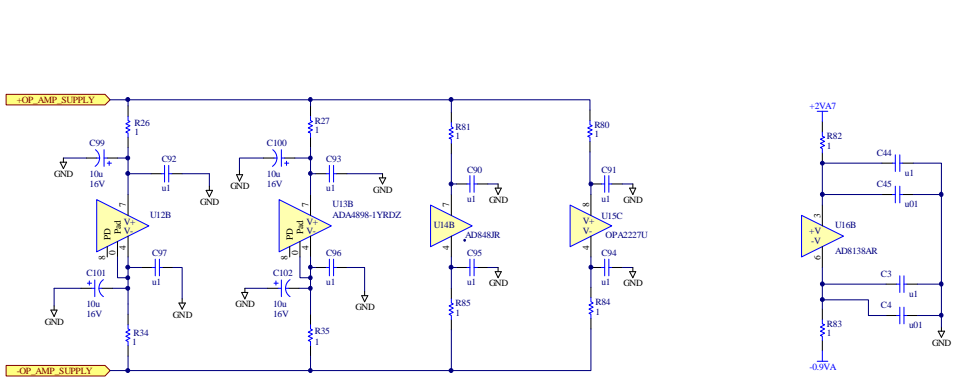
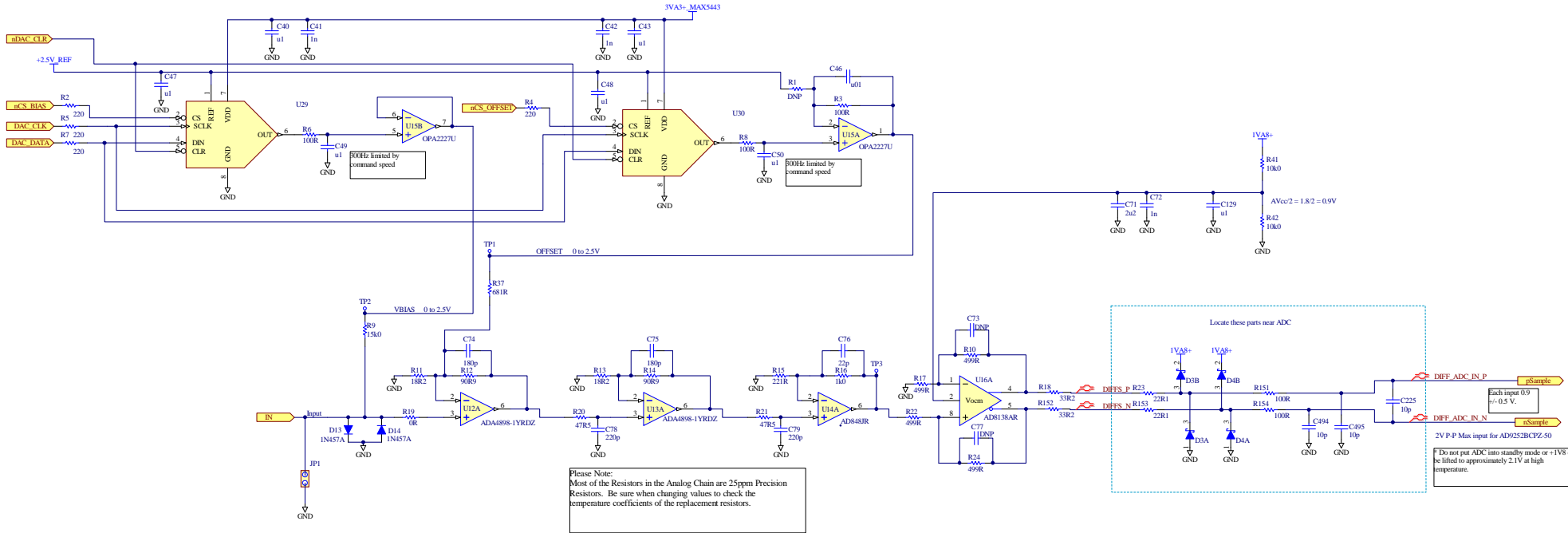


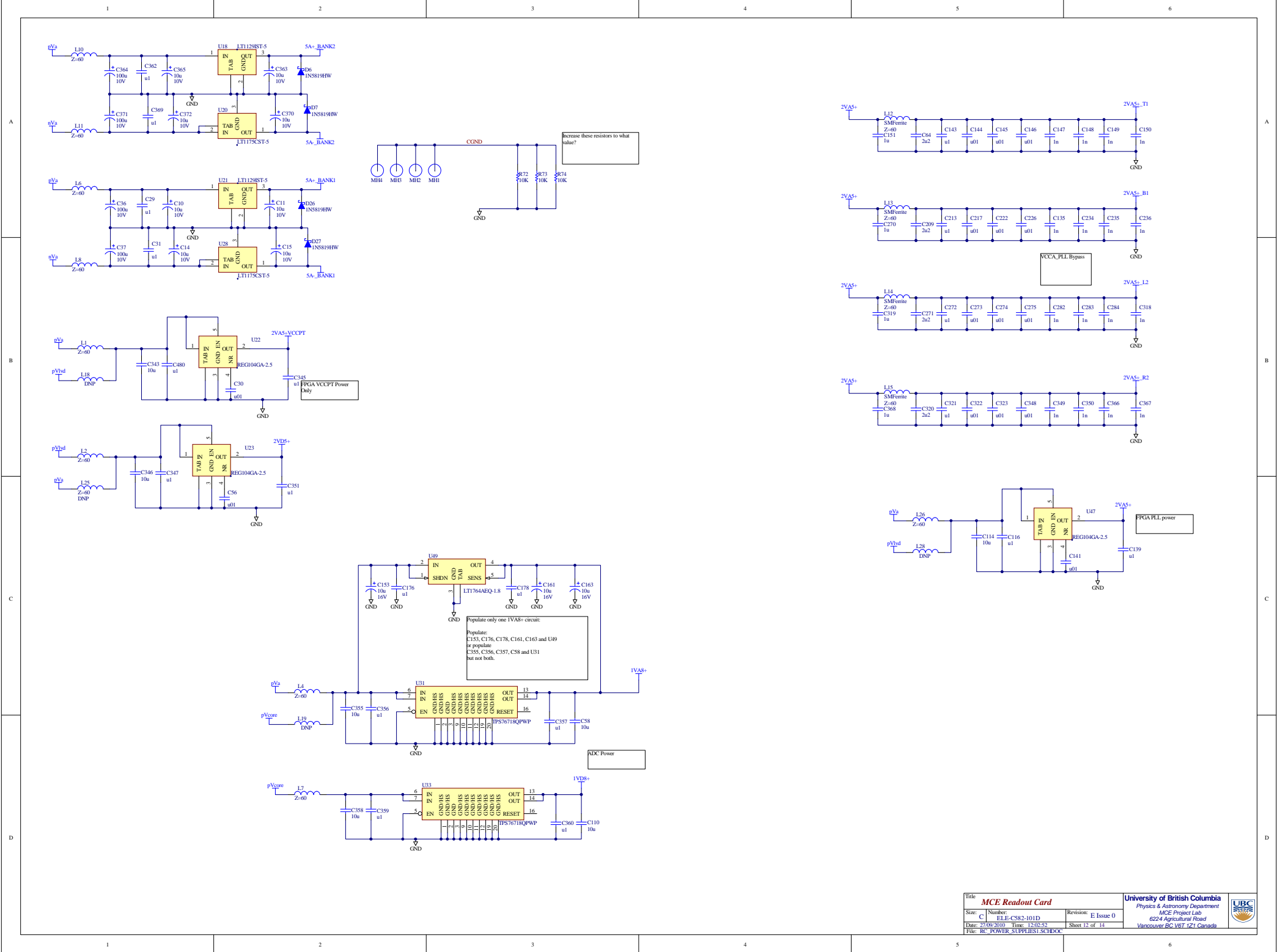




Locate terminations close to DDR IC. Termination capacitances will need to be adjusted empirically.







A

B

C

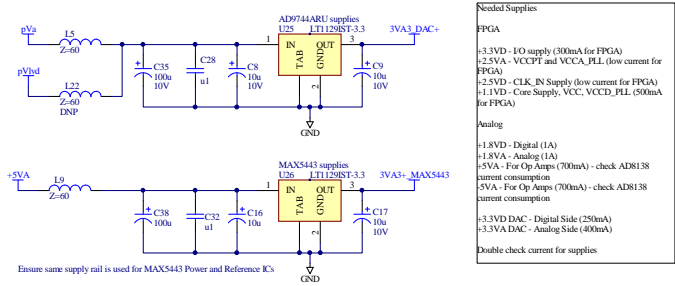
D

A

B

C

D



Needed Supplies

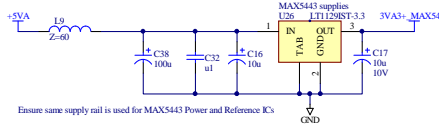
FPGA

- +3.3VD - I/O supply (300mA for FPGA)
- +2.5VA - VCCPT and VCCA_PLL (low current for FPGA)
- +2.5VD - CLK_IN Supply (low current for FPGA)
- +1.1VD - Core Supply, VCC, VCCD_PLL (500mA for FPGA)

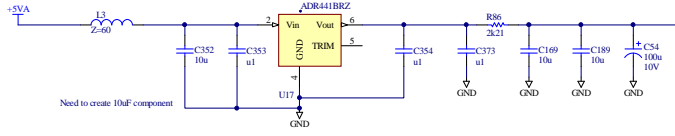
Analog

- +1.8VD - Digital (1A)
- +1.8VA - Analog (1A)
- +5VA - For Op Amps (700mA) - check AD8138 current consumption
- +5VA - For Op Amps (700mA) - check AD8138 current consumption
- +3.3VD DAC - Digital Side (250mA)
- +3.3VA DAC - Analog Side (400mA)

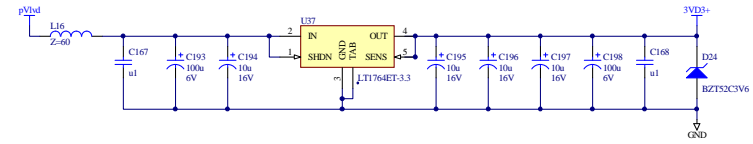
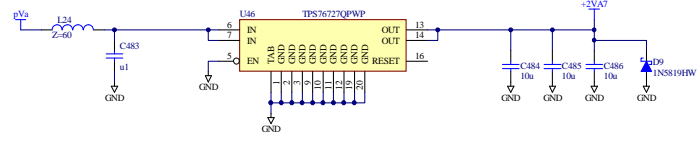
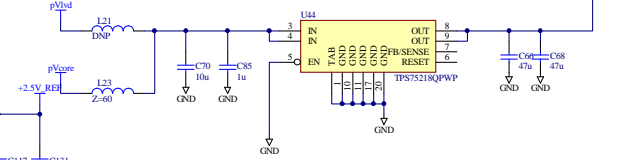
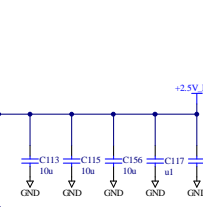
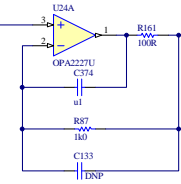
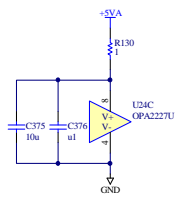
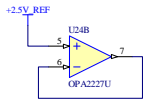
Double check current for supplies



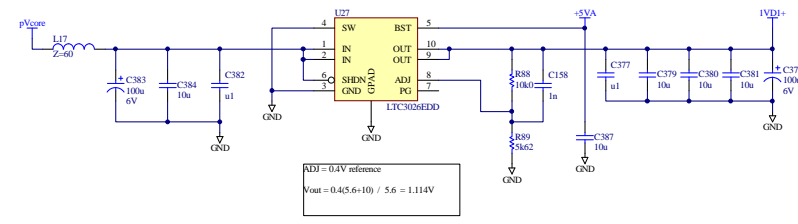
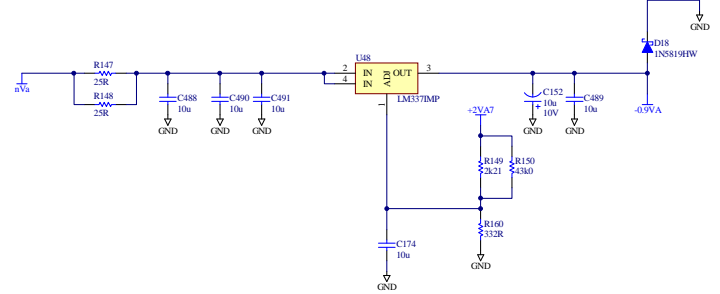
Ensure same supply rail is used for MAX5443 Power and Reference ICs



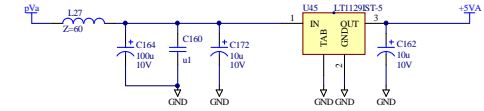
Need to create 10uF component



VCC Supplies



ADI = 0.1V reference
 $V_{out} = 0.45 \cdot 6 \cdot 10 / 5.6 = 1.114V$



1

2

3

4

5

6

A

A

B

B

C

C

D

D

Front Panel Mounting Assembly

Bottom Extraction Handle
 Manufacturer: Rittal
 Part Number: 3686-902
 Mech3

Top Extraction Handle
 Manufacturer: Rittal
 Part Number: 3686-903
 Mech4

SCUBA2 Readout Card Front Panel
 Manufacturer: PHAS-MS
 Part Number: SC2-ELE-S581-110
 Mech8

Mounting Bracket for PCB
 Manufacturer: Rittal
 Part Number: 3685-198 (10/pack)
 Mech11

Mounting Bracket for PCB
 Manufacturer: Rittal
 Part Number: 3685-198 (10/pack)
 Mech12

M2.5 x 8mm Machine Screw Cone Head
 Type: Hardware
 Mech15

M2.5 x 8mm Machine Screw Cone Head
 Type: Hardware
 Mech16

M2.5 x 8mm Machine Screw
 Type: Hardware
 Mech19

M2.5 x 8mm Machine Screw
 Type: Hardware
 Mech20

M2.5 x 8mm Machine Screw
 Type: Hardware
 Mech21

M2.5 x 8mm Machine Screw
 Type: Hardware
 Mech22

Title		
Size B	Number	Revision
Date: 27/09/2010	Sheet of	
File: C:\docs\ARC_Mechanical.SchDoc	Drawn By:	

1

2

3

4

5

6