COMMON-USER
SCUBA2
SUBMILLIMETRE
ARRAY - 2

Bus backplane

Clock Card

On-board
JTAG header

JTAG port

EPC16
Factory
Configuration
Device

Configuration
Interface

Flash
Interface

SRAM
2M (min)

Logic

EPC16
Application
Configuration
Device

JTAG port

Configuration port

Stratix FPGA

Jam in

Jam out

JTAG_SEL

JTAG in

JTAG out

Fibre Optic
Interface

Control 0, Byte Blaster Enabled 1, Jam Enabled

Logic

nByteBEn
(manual
switch)

Faceplate JTAG header

Other Card

Bypass disable
when card inserted

JTAG port

Configuration port

Configuration
interface

JTAG port

EPC16
Configuration
device

Stratix FPGA

FLASH
interface

Last Card

Bypass disable
when card inserted

JTAG port

Configuration port

Configuration
interface

JTAG port

EPC16
Configuration
device

Stratix FPGA

FLASH
interface

JTAG chain

Control Lines

UBC
University of British Columbia
Physics and Astronomy Dept.

Title
FPGA Configuration Block Diagram

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Drawn by BNB   Sheet 1 of 1