clock\clock\struct

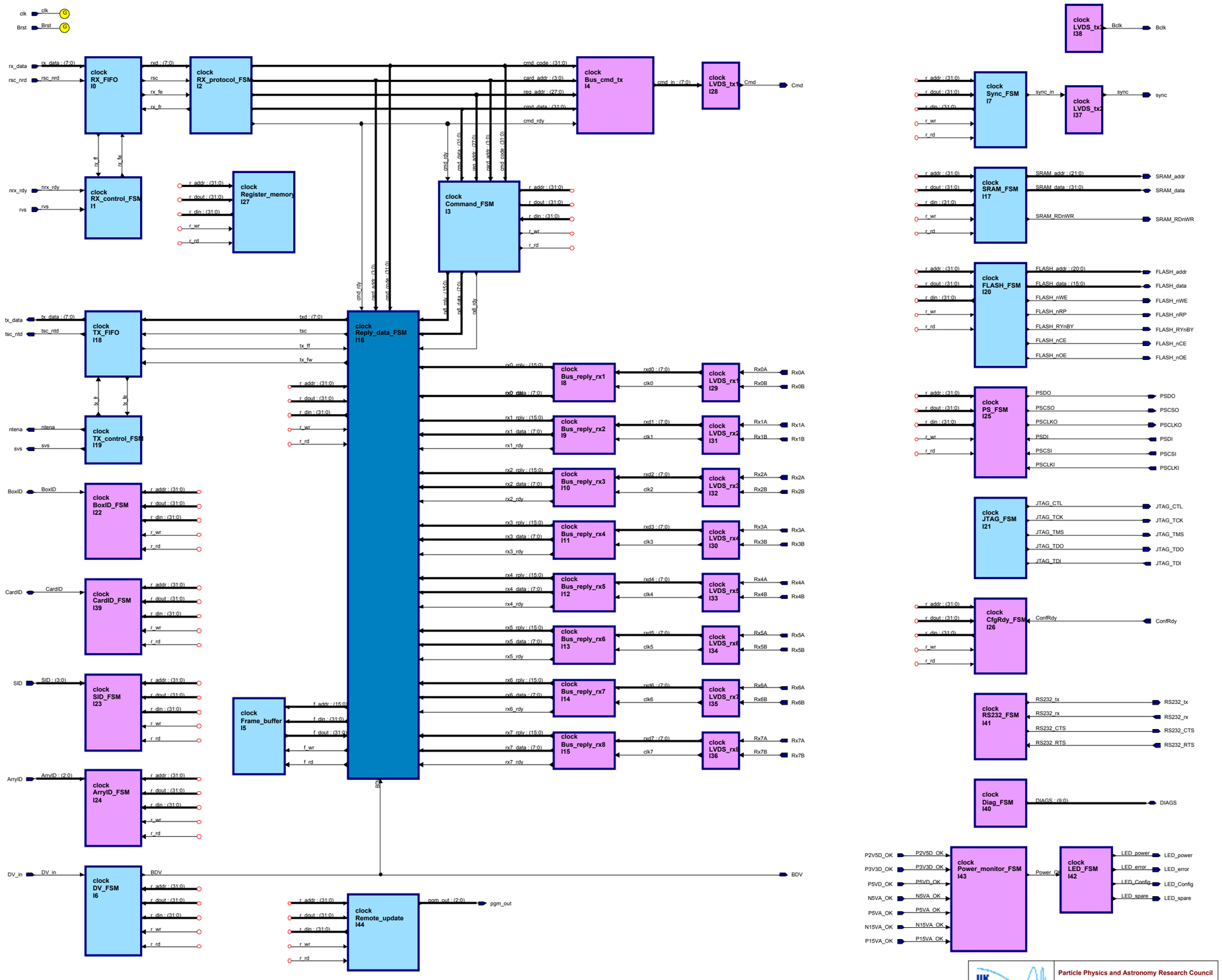
Package List
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;

Declarations
Ports:

```
ArryID       : std_logic_vector(2 DOWNTO 0)
Brst         : std_logic
ConfRdy      : std_logic
DV_in        : std_logic
JTAG_TDI     : std_logic
N15VA_OK     : std_logic
N5VA_OK      : std_logic
P15VA_OK     : std_logic
P2V5D_OK     : std_logic
P3V3D_OK     : std_logic
P5VA_OK      : std_logic
P5VD_OK      : std_logic
PSCLKI       : std_logic
PSCSI        : std_logic
PSDI         : std_logic
RS232_RTS    : std_logic
RS232_rx     : std_logic
Rx0A         : std_logic
Rx0B         : std_logic
Rx1A         : std_logic
Rx1B         : std_logic
Rx2A         : std_logic
Rx2B         : std_logic
Rx3A         : std_logic
Rx3B         : std_logic
Rx4A         : std_logic
Rx4B         : std_logic
Rx5A         : std_logic
Rx5B         : std_logic
Rx6A         : std_logic
Rx6B         : std_logic
Rx7A         : std_logic
Rx7B         : std_logic
SID          : std_logic_vector(3 DOWNTO 0)
clk          : std_logic
nrx_rdy      : std_logic
rsc_nrd      : std_logic
rvs          : std_logic
rx_data      : std_logic_vector(7 DOWNTO 0)
BDV          : std_logic
Bclk         : std_logic
Cmd          : std_logic
FLASH_RYnBY  : std_logic
FLASH_addr   : std_logic_vector(20 DOWNTO 0)
FLASH_nCE    : std_logic
FLASH_nOE    : std_logic
FLASH_nRP    : std_logic
FLASH_nWE    : std_logic
JTAG_CTL     : std_logic
JTAG_TCK     : std_logic
JTAG_TDO     : std_logic
JTAG_TMS     : std_logic
LED_Config   : std_logic
LED_error    : std_logic
LED_power    : std_logic
LED_spare    : std_logic
PSCLKO       : std_logic
PSCSO        : std_logic
PSDO         : std_logic
RS232_CTS    : std_logic
RS232_tx     : std_logic
SRAM_RDnWR   : std_logic
SRAM_addr    : std_logic_vector(21 DOWNTO 0)
ntena        : std_logic
PGM_out      : std_logic_vector(2 DOWNTO 0)
svs          : std_logic
sync         : std_logic
tsc_ntd      : std_logic
tx_data      : std_logic(7 DOWNTO 0)
BoxID        : std_logic
CardID       : std_logic
DIAGS        : std_logic_vector(9 DOWNTO 0)
FLASH_data   : std_logic_vector(15 DOWNTO 0)
SRAM_data    : std_logic_vector(31 DOWNTO 0)
```

Diagram Signals:

```
SIGNAL Power_OK     : std_logic
SIGNAL card_addr    : std_logic_vector(3 DOWNTO 0)
SIGNAL clk0         : std_logic
SIGNAL clk1         : std_logic
SIGNAL clk2         : std_logic
SIGNAL clk3         : std_logic
SIGNAL clk4         : std_logic
SIGNAL clk5         : std_logic
SIGNAL clk6         : std_logic
SIGNAL clk7         : std_logic
SIGNAL cmd_code     : std_logic_vector(31 DOWNTO 0)
SIGNAL cmd_data     : std_logic_vector(31 DOWNTO 0)
SIGNAL cmd_in       : std_logic_vector(7 DOWNTO 0)
SIGNAL cmd_rdy      : std_logic
SIGNAL f_addr       : std_logic_vector(15 DOWNTO 0)
SIGNAL f_din        : std_logic_vector(31 DOWNTO 0)
SIGNAL f_dout       : std_logic_vector(31 DOWNTO 0)
SIGNAL f_rd         : std_logic
SIGNAL f_wr         : std_logic
SIGNAL r_addr       : std_logic(31 DOWNTO 0)
SIGNAL r_din        : std_logic(31 DOWNTO 0)
SIGNAL r_dout       : std_logic(31 DOWNTO 0)
SIGNAL r_rd         : std_logic
SIGNAL r_wr         : std_logic
SIGNAL reg_addr     : std_logic_vector(27 DOWNTO 0)
SIGNAL rsc          : std_logic
SIGNAL rx0_data     : std_logic_vector(7 DOWNTO 0)
SIGNAL rx0_rdy      : std_logic
SIGNAL rx0_rply     : std_logic_vector(15 DOWNTO 0)
SIGNAL rx1_data     : std_logic_vector(7 DOWNTO 0)
SIGNAL rx1_rdy      : std_logic
SIGNAL rx1_rply     : std_logic_vector(15 DOWNTO 0)
SIGNAL rx2_data     : std_logic_vector(7 DOWNTO 0)
SIGNAL rx2_rdy      : std_logic
SIGNAL rx2_rply     : std_logic_vector(15 DOWNTO 0)
SIGNAL rx3_data     : std_logic_vector(7 DOWNTO 0)
SIGNAL rx3_rdy      : std_logic
SIGNAL rx3_rply     : std_logic_vector(15 DOWNTO 0)
SIGNAL rx4_data     : std_logic_vector(7 DOWNTO 0)
SIGNAL rx4_rdy      : std_logic
SIGNAL rx4_rply     : std_logic_vector(15 DOWNTO 0)
SIGNAL rx5_data     : std_logic_vector(7 DOWNTO 0)
SIGNAL rx5_rdy      : std_logic
SIGNAL rx5_rply     : std_logic_vector(15 DOWNTO 0)
SIGNAL rx6_data     : std_logic_vector(7 DOWNTO 0)
SIGNAL rx6_rdy      : std_logic
SIGNAL rx6_rply     : std_logic_vector(15 DOWNTO 0)
SIGNAL rx7_data     : std_logic_vector(7 DOWNTO 0)
SIGNAL rx7_rdy      : std_logic
SIGNAL rx7_rply     : std_logic_vector(15 DOWNTO 0)
SIGNAL rx8_data     : std_logic_vector(7 DOWNTO 0)
SIGNAL rx8_rdy      : std_logic
SIGNAL rx8_rply     : std_logic_vector(15 DOWNTO 0)
SIGNAL rx_fe        : std_logic
SIGNAL rx_ff        : std_logic
SIGNAL rx_fr        : std_logic
SIGNAL rx_fw        : std_logic
SIGNAL rxd          : std_logic_vector(7 DOWNTO 0)
SIGNAL rxd0         : std_logic_vector(7 DOWNTO 0)
SIGNAL rxd1         : std_logic_vector(7 DOWNTO 0)
SIGNAL rxd2         : std_logic_vector(7 DOWNTO 0)
SIGNAL rxd3         : std_logic_vector(7 DOWNTO 0)
SIGNAL rxd4         : std_logic_vector(7 DOWNTO 0)
SIGNAL rxd5         : std_logic_vector(7 DOWNTO 0)
SIGNAL rxd6         : std_logic_vector(7 DOWNTO 0)
SIGNAL rxd7         : std_logic_vector(7 DOWNTO 0)
SIGNAL sync_in      : std_logic
SIGNAL tsc          : std_logic
SIGNAL tx_fe        : std_logic
SIGNAL tx_ff        : std_logic
SIGNAL tx_fr        : std_logic
SIGNAL tx_fw        : std_logic
SIGNAL txd          : std_logic(7 DOWNTO 0)
```



UK Astronomy Technology Centre	Particle Physics and Astronomy Research Council Royal Observatory Edinburgh		
Title:	Clock card	Drawing no:	SC2_ELE_S563_200
Path:	clock/clock/struct	Revision:	01
Edited:	by mae on 05 Jun 2003	Sheet:	1 of 1